Logic Analysis Basics

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presented by:

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Introduction

If you have ever asked yourself these questions:

- What is a logic analyzer?
- What is a timing/state analyzer?
- What is a trigger?
- When should I use a logic analyzer?

Then you are in the RIGHT place!!!
Agenda

• Overview of a Logic Analyzer
• Logic Analyzer Process
  – Connect (Probing)
  – Acquire
    • Timing Analyzer
    • State Analyzer
  – Data Analysis Tools and Display
• Conclusion
Logic Analyzer is a Tool that:

Gives you insight into the operation of a *digital* circuit by
- Connecting to your DUT (Device Under Test)
- Capturing and storing the digital waveforms
- Analyzing the stored data and displaying the results.
What Can a Logic Analyzer Do for Me?

- Record a circuit’s logic levels over time, and let you examine the record
- Show whether or not a particular event happens (the trigger)
- Provide a precise measure of time between events
- Inverse-assemble a microprocessor’s logic levels to tell you what code was running
- Analyze complex buses and protocols
Logic Analysis Process

Critical Factors

Logic Analysis Process

Features & Tools

• Soft Touch Connectorless
• Samtec
• Mictor
• Analysis Probes
• Flying Leads
• FPGA Dynamic Probe

Probing

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Logic Analysis Process

**Critical Factors**
- Accurate & robust measurements

**Logic Analysis Process**
- Connect
- Acquire

**Features & Tools**
- Soft Touch Connectorless
- Samtec
- Mictor
- Analysis Probes
- Flying Leads
- FPGA Dynamic Probe
- Bus Speeds
- Depth
- Card Configuration
Logic Analysis Process

Critical Factors

Logic Analysis Process

Features & Tools

Connect

Probing

Acquire

Accurate & robust measurements

Present Data

Data analysis and signal integrity insight

• Soft Touch Connectorless
• Samtec
• Mictor
• Analysis Probes
• Flying Leads
• FPGA Dynamic Probe

• Bus Speeds
• Depth
• Card Configuration

• Software Analysis
• Protocol Analysis
• Inverse Assembly
• State Display
• Timing Display
• Eye Diagrams

Accurate & robust measurements

Data analysis and signal integrity insight

Software Analysis

Protocol Analysis

Inverse Assembly

State Display

Timing Display

Eye Diagrams

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It Begins At The Probe…

General-purpose probing

Designed into the target

Application-specific probes

Connect  Acquire  Present

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Electrical Probing Considerations

• How can I connect to my signals?
  – Design-in connector
  – Flying leads

• Low loading
  – System tolerance
  – Impact on DUT
Mechanical Probing Considerations

• What can I fit on my board?
  – Footprint size
  – Signal routing
  – Low profile

• Usable
  – Easy to attach
  – Reliable, repeatable
Understanding Logic Analyzer Specifications

**Memory Depth:** specifies how many samples can be stored in a single trace.

**Max Timing Rate:** The fastest speed of the internal sampling clock

**Max State Clock Rate:** The fastest, externally input, state clock allowed

**Channel Count (Width):** How many signals can be stored per sample
Logic Analyzer Setup

Assign bus/signal names

Assign channels to buses/signals

Assign voltage threshold

Connect
Acquire
Present

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Acquire - Two Measurement Modes

Timing Analysis
(Logic Timing)

State Analysis
(Logic Events)
Acquire - Two Measurement Modes

Timing Analysis
(Logic Timing)

State Analysis
(Logic Events)
Timing Mode (Asynchronous)

- Tells *when* the event happened
- Displays signal edge timing relationships
- Trigger across multiple channels
- Analogous to an oscilloscope with 1-bit resolution
- Useful for hardware debug

Asynchronous – Sampling clock comes from internal logic analyzer
Timing Mode – How it Works

Connect

Acquire

Present
Timing Waveform
When to Use an Oscilloscope

- Parametric Measurements
- Precise Time vs. Voltage Relationships

Diagram:
- Overshoot
- Valid Logic 1
- Rise
- Droop
- Ringing
- Pulse Width
- Valid Logic 0
- Rise Time
- Fall Time

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When to Use a Logic Analyzer

- Cause and effect timing relationships
- Many channels simultaneously
- Multiple bus correlation measurements
High Speed Timing Zoom

- Efficiently characterize hardware with 250ps resolution
- Useful at high speeds
- Capture simultaneously with traditional timing or state measurements
- Provides a window of visibility around the trigger

Up to 4 GHz timing speeds at 64k memory depth
Transitional Sampling

- Only stores transitions
- Utilize memory efficiently
- Two memory locations per transition

Signal being acquired

Sampling points

Transitional storage

Connect  Acquire  Present

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Acquire - Two Measurement Modes

Timing Analysis
(Logic Timing)

State Analysis
(Logic Events)
State Analysis (Synchronous)

• Useful for determining *what* happened – sequence of operations
• Trace values on a bus
• Track functional problems and code flow
• Useful for software debug and hardware/software integration

Synchronous – Sampling clock comes from device under test (DUT)
State Analysis: Data Valid Window

- Definition: Period of time in which data is stable
  - Setup time – the time data is stable prior to clock edge
  - Hold time – the time data is stable following clock edge
State Analysis: Setup and Hold Example

- Setup Time
- Hold Time
- DUT Clock
- D Flip Flop
- Setup Time
State Analysis: State Domain

<table>
<thead>
<tr>
<th>Clock</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>AA</td>
</tr>
<tr>
<td>2</td>
<td>0C</td>
</tr>
<tr>
<td>3</td>
<td>B3</td>
</tr>
</tbody>
</table>
State Analysis: Eye Finder

- Immediate confirmation and confidence in sampled data!
  - Automatic placement of sample position in the data valid region
  - Easy to modify manually
  - Quick overview of target signal skew
State Analysis: Synchronous Measurement

- **Input** $V_{\text{Input}}$
- **Comparator**
- **Output** $(0 \text{ or } 1)$
- **Latch**
- **Output** $V_{\text{Output}}$
- **External DUT Clock**
- **DUT**

**Threshold**
State Analysis: State Listing

- Trace values on a bus (see data values your device sees)
- Track functional problems and code flow

<table>
<thead>
<tr>
<th>Label&gt;</th>
<th>ADDR</th>
<th>DATA</th>
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<th>SYMB</th>
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<td>HEX</td>
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<td></td>
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<tr>
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<td>00</td>
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<td></td>
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Circuit Measurement

Connect Acquire Present

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State Analysis: Displaying State Measurements

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<th>Sample Number</th>
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<th>DATA</th>
<th>OE_WE</th>
<th>Time</th>
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<td>13</td>
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<tr>
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Click here for trigger menu

[Logos: Agilent Technologies]
State Analyzers

Ideal for Analyzing the Execution of Microprocessor Programs

Measurement Channel

Clock Signal

Start

n = 0

n = n + 1

n > 15

No

Yes

End

DUT

Connect

Acquire

Present

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Triggering
The Conveyor Belt Analogy

One Sample = One box
Acquired Samples = Boxes on the belt
Memory Depth = Number of boxes that will fit on the belt
Trigger Position = Position of special box when Stop button is pressed
A Trigger is an event that, when detected, allows the logic analyzer to fill its trace memory and complete the measurement.
Single-Shot View of System

Trace Memory

Captured Activity

System Activity

Display Tool

More memory provides longer acquisition window (seconds)
## Trigger Positions

<table>
<thead>
<tr>
<th>Trigger Position</th>
<th>Use of Trigger</th>
</tr>
</thead>
<tbody>
<tr>
<td>Start</td>
<td>Observe code execution</td>
</tr>
<tr>
<td>Center (Default)</td>
<td>View time shortly before/after event</td>
</tr>
<tr>
<td>End</td>
<td>Trace cause of system halt Root cause analysis (uncorrelated symptoms)</td>
</tr>
<tr>
<td>0-100%</td>
<td>Variable, custom selection</td>
</tr>
</tbody>
</table>
Defining Trigger Events

Measurement Channel Input

Acquisition Buffer

Display Buffer

Trigger Enable Function

Logic Analyzer Control

Connect
Acquire
Present

Trigger Event

D4 ... D0
1 0 0 0 1
0 0 0 1 0
0 0 1 0 1

1 0 0 0 1
0 0 0 1 0
0 0 1 0 1

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Defining Simple Trigger Events

Trigger on Bus values

Trigger on Signal values
Defining Advanced Trigger Events

Find an edge occurring coincidentally with a bus pattern.
The Complete Measurement

Diagram showing the Complete Measurement process:
- DUT (Device Under Test)
- Comparator
- Latch
- Clock Signal
- Acquisition Buffer
- Trigger Enable Function
- Display Buffer
- Logic Analyzer Control
- Connect
- Acquire
- Present

Binary representation:
- D6: 1001101
- D5: 1010101
- D4: 1100101
- D3: 1001101
- D2: 1010101
- D1: 1100101
- D0: 1100101
Displaying the Data

There are a number of ways to display the 1’s and 0’s to make sense of your digital design:

- Waveform
- Listing
- View Scope
- Inverse Assembly, Source Correlation
- Protocol Debug / Packet Viewer
- Eye Diagrams – Eye Scan
- Custom Views – with custom VBA Views
- Digital VSA
View Scope

- Import oscilloscope waveforms with time-correlated global markers
- Track errors through analog and digital
- Analyze analog characteristics of digital anomalies
Scope triggered to find max distortion with G1 and G2 markers positioned at start and end of first flat distortion.
Inverse Assembly: Listing Correlated to Waveform at G1

<table>
<thead>
<tr>
<th>PC</th>
<th>MPC821/860 Inverse Assembler</th>
</tr>
</thead>
<tbody>
<tr>
<td>Symbols</td>
<td>10=hex, 10.=decimal, %10=binary</td>
</tr>
</tbody>
</table>

| /q.elf:reset+0420 | subi r1 r1 0018 |
| /q.elf:reset+0424 | stmw r26 0000(r1) |
| /q.elf:reset+0428 | mfmsr r26 |
| /q.elf:reset+042c | ori r26 r26 0002 |
| /q.elf:reset+0430 | mtmsr r26 |
| /q.elf:reset+0434 | subi r1 r1 0008 |
| /q.elf:reset+0438 | bl q::isr::ext_exception |
| | isr::ext_exception |
| | mfspr r0 lr |
| ext_exceptio+0004 | stw r0 0004(r1) |
| ext_exceptio+0008 | stwu r1 FFF8(r1) |
| ext_exceptio+000c | lis r12 0000 |

State listing reveals code branching just prior to G1.
Between G1 and G2 D/A execution is interrupted when code goes to interrupt service routine. Line 55 correlated to G1 marker in state listing and waveform.
Protocol Analysis: Packet Viewer

- Displays parallel bus data at protocol level
- Protocol trigger macro allows easy trigger setup, eliminates manual configuration of complex measurements
- Time correlation with other system buses
- Coverage includes:
  - Rapid IO
  - PCIE Express
  - USB
  - Serial ATA
  - Proprietary/Custom Protocols
Eye Diagrams: Eye Scan

• What is Eye Scan?

• Provides signal integrity validation measurements of entire high-speed buses.

• Uses high resolution comparators to scan across specified time and voltage range.

• Provides up to 5mV and 10ps resolution.

• Can be used as a tool of “first attack” to reveal tough signal integrity problems.
FPGA Dynamic Probe

- Insert ATC2 core with Xilinx Core Inserter
- Control access to new signals via JTAG
- JTAG
- FPGA Dynamic Probe SW application supported by 1680/1690/16900
- Probe core output
- Agilent Technologies
Summary
# Using a Logic Analyzer vs. an Oscilloscope

<table>
<thead>
<tr>
<th>Use a Logic Analyzer to:</th>
<th>Use an Oscilloscope:</th>
</tr>
</thead>
<tbody>
<tr>
<td>See many signals at once</td>
<td>To get precise time interval information</td>
</tr>
<tr>
<td>Look at signals the same way your hardware does (State Mode)</td>
<td>To look at the analog characteristics of a signal</td>
</tr>
<tr>
<td>Trigger on a pattern of highs and lows on several lines and see the result</td>
<td></td>
</tr>
<tr>
<td>Verify timing relationships among several or hundreds of lines (Timing Mode)</td>
<td></td>
</tr>
</tbody>
</table>
State vs. Timing

- **Timing Analysis**
  - When the event happened
  - Edge relationships
  - Hardware debug

- **State Analysis**
  - What sequence of operations executed
  - Monitor execution of processor
  - Software and System Integration
Common Applications for Logic Analyzers

- Intel FSB
- DDR/DDR2/DDR3
- Fully Buffered DIMM
- PCI Express
- Digital Radio – Digital I&Q
- SATA/SAS
- InfiniBand
- RapidIO
- SPI 4.2
- Fibre Channel
- USB 2.0
- IEEE 1394
- FPGA Functional Verification
- Other µP
Multiple Views Provide the Right Level of Insight

System Performance

Eye Scan

Listing & IA

Oscilloscope

Waveform

Digital VSA

Packet Decode

Source Code

Connect

Acquire

Present

Agilent Technologies
Introducing Agilent 16800 series

Logic Analyzer
- **4 GHz Timing Zoom** @ 64K deep
- Up to **1 GHz timing** with deep memory
- Up to **450 MHz state** clock rate
- Up to **500 Mb/s state data rate**
- Up to **32 M deep memory**
- compatible with 19 years of **legacy probing** + newest **connectorless probing** innovations

Pattern Generator:
- **48 channels**
- Up to **16 M vectors** deep,
- Up to **300 Mb/s**

![Image of Agilent 16800 series Logic Analyzer and Pattern Generator]

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Q & A