Charge-Borrowing Decap: A Novel Circuit for Removal of Local Supply Noise Violations

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Abstract- We propose a novel circuit called charge-borrowing decap (CBD) as a drop-in replacement for passive decaps to reduce supply noise for removal of “hot-spot” IR-drop problems found late in the design process. Measurement results on a 90nm test chip show that a noise reduction improvement between 42%-55% at 100MHz-1.5GHz over its passive counterpart.

I. INTRODUCTION

The increase in clock frequency and on-chip current demand makes power grid design a challenging task. Decoupling capacitors (decaps) are generally used to reduce IR drop and Ldi/dt effects, and hence keep the power supply relatively constant. Starting from 90nm, simply placing passive decaps in the available open areas of the chip may not be sufficient [1]. Large power supply noise levels in localized regions (called “hot spot” IR-drop violations) may unexpectedly be present in high-speed applications. These unresolved hot spots cause timing closure problems or result in functional failures in extreme cases. To remove them, active decaps [2][3][4] have been proposed for use as a drop-in replacement of the passive decaps. The use of active decaps saves time and effort near the tapeout deadline, and therefore provides an attractive solution. This paper proposes a novel charge-borrowing decap (CBD). The CBD design provides significantly more charge than a passive decap to reduce the local supply noise level, with only a minimum power loss during charge transfer from a clean supply node. As a result, the new circuit provides better noise reduction performance than passive decaps and even active decaps. With a relatively simple and robust design, the CBD only requires a small area overhead.

II. CHARGE-BORROWING DECAP CONCEPT AND DESIGN

A. Charge-Borrowing Decap Concept

![Diagram of CBD and Passive Decap](image)

Fig. 1. CBD concept shown in (b), compared to a passive decap in (a).

The main purpose of a decap is to provide charge to stabilize the supply voltage locally. Unlike a passive decap, which provides charge from itself, our new circuit “borrows” charge from a clean supply node to reduce local noise level. This charge borrowing is accomplished using the effect of capacitive feedthrough, as illustrated in Fig. 1. For a fixed decoupling capacitance of $C_{\text{decap}}$, we assume certain supply noise $kV_{\text{DD}}$ is present on the supply, where $k$ is a fractional number and normally in the range of 0.05 to 0.2. A passive decap, as shown in Fig. 1(a), provides a charge of $kC_{\text{decap}}V_{\text{DD}}$ to the supply. In a CBD, as shown in Fig. 1(b), however, the charge provided by the CBD circuit in one clock cycle can ideally be up to $C_{\text{decap}}\Delta V_{\text{clk}} = C_{\text{decap}}V_{\text{DD}}$, where $\Delta V_{\text{clk}}$ is the clock swing. Clearly, over one clock cycle, the CBD provides 5X-20X more charge than a same-area passive decap, depending on the actual noise level. From another perspective, the CBD circuit can boost the local supply voltage to $2V_{\text{DD}}$ ideally, but passive decaps cannot.

The circuit in Fig. 1(b) suffers from clock feedthrough problems on the falling edge of the clock. When the Clk signal rises from 0 to $V_{\text{DD}}$, the supply is boosted to $2V_{\text{DD}}$ ideally due to capacitance feedthrough. Then, nearby user logic circuits switch, resulting in certain amount of charge to withdraw from the supply, reducing the supply voltage by $\Delta V$. When the Clk signal falls from $V_{\text{DD}}$ back to 0, the supply voltage drops from $2V_{\text{DD}}-\Delta V$ to $V_{\text{DD}}-\Delta V$, which may not be acceptable if $\Delta V$ is large. This problem can be solved by adding additional circuitry as shown in Fig. 2(a). Two diodes are inserted at node B1, one connected to the clean supply and the other to the noisy supply. Without the connection to the clean $V_{\text{DD}}$, when the clock is low, B1 stays at roughly $V_{\text{SS}}$ since the current flow from $V_{\text{DD}}$ to B1 is prevented by the diode, D2. When the clock goes high, B1 rises to $V_{\text{DD}}$. This boost in voltage will not trigger current flow from B1 to the supply because both B1 and the supply are at the same level ($-V_{\text{DD}}$). Thus, the voltage at B1 should be around $V_{\text{DD}}$ when the clock is low. This ensures that the voltage at B1 can reach about $2V_{\text{DD}}$ when the clock goes high and the noisy supply can be charged. To achieve that, access to a clean supply of $V_{\text{DD}}$ is needed through D1.

![Diagram of Diode Inserted CBD and MOS Implementation](image)

Fig. 2. (a) Diode inserted CBD and (b) one possible MOS implementation.

Assuming there is one threshold voltage $V_T$ drop across each diode, the operation of the CBD circuit, as illustrated in Fig. 2(a), is follows. When Clk is at 0, the noisy supply node is assumed to be at $V_{\text{DD}}$, while B1 is charged at $V_{\text{DD}}-V_T$ from the clean supply. When Clk rises to $V_{\text{DD}}$, B1 rises to $2V_{\text{DD}}-V_T$ at the same time. As a result, the noisy supply node is...
increased to $2V_{DD}-2V_T$. Before the clock falls, the noisy supply drops by $\Delta V$ to $2V_{DD}-2V_T-\Delta V$. Then, Clk falls back to 0, and B1 is reduced to $V_{DD}-V_T$. However, D2 prevents charge from flowing back to B1 from the supply. Therefore, the noisy supply remains at $2V_{DD}-2V_T-\Delta V$.

In a CMOS process, the diodes shown in Fig. 2(a) can be implemented as in Fig. 2(b). When the clock is low, B2 is set at $V_{SS}$, which allows B1 to be charged to $V_{DD}$. The higher gate voltage of B2 at $2V_{DD}$ avoids forward-biasing the pn junction of Mdp1 and increases the B1 voltage from $2V_{DD}+|V_{thp1}|$ to $2V_{DD}$, where $|V_{thp1}|$ is the threshold voltage of Mdp1. When B1 rises, it causes current flow to charge the noisy supply rail. Assuming that the supply is localized, then the boosted voltage is $2V_{DD}+|V_{thp2}|$ due to the threshold voltage degradation of Mdp2. Note that in Fig. 2(b), the gate-body voltages of both transistors Mdp1 and Mdp2 are always within one $V_{DD}$ of each other, ensuring gate-oxide reliability.

To generate the bootstrapped signal at node B2, a clock multiplier [5][6] can be used, as shown in Fig. 3. Due to leakage through the transistors, it can be verified that both nodes B3 and B4 are at roughly $V_{DD}$ while both transistors Mcn1 and Mcn2 are shut off. When the clock goes low, B3 goes to $2V_{DD}$ and B4 is at $V_{DD}$, which causes Mcn2 to turn on. The output node B2 is low, along with the clock signal. When the clock rises to $V_{DD}$, B3 is discharged from $2V_{DD}$ to $V_{DD}$, whereas B4 is charged up to $2V_{DD}$. This causes Mcn1 to turn on and Mcn2 to turn off. The rise of the clock signal also turns on Mip, allowing the output node B2 to follow B4. Because the gate of Mip is at $V_{SS}$, the voltage at B2 can rise to $2V_{DD}$ without any voltage loss. Similar to the previous approach, the body of the transistor Mip is connected to B4 to ensure reverse-biased pn junctions. For Mcn1 and Mcn2, thick-oxide transistors are used to reduce the risk of oxide breakdown because their gate-body voltages can be as high as $2V_{DD}$.

### B. “Clk” Signal Generation

A critical concern about the charge-borrowing decap design is the additional capacitive loading on the clock distribution system if the main clock of the chip is connected to the Clk input of the CBD. Since the CBD has a large capacitance in the range of picofarads, such a large capacitor loaded on the clock tree may cause an imbalance of the tree and introduce more clock skew and jitter [7]. In extreme cases, this extra loading may cause a functional failure in the clock distribution network. Therefore, the Clk input of the CBD should be generated from some other sources to keep the main clock tree unaffected.

We use a simple ring oscillator to generate the Clk signal, as illustrated in Fig. 4. A total of 39 inverter stages were used to provide an oscillation frequency of 1GHz. If the chip’s operating frequency is below 1GHz, the design does not harm the logic circuits connected to the local supply as long as the slew rate of the boosted voltages remains controlled within practical limitations. The ring oscillator uses unit-sized inverters and consumes 65$\mu$W of dynamic power. To provide enough current flow to charge and discharge the decoupling capacitor $C_{decap}$ in the CBD, a chain of inverters was added and sized according to logical effort. A fan-out factor of the inverter chain was selected to be about 3-4 so that the delay through the chain was minimized. The number of stages required to generate the fan-out factor was then calculated. Of course, the circuit in Fig. 4 will cause additional supply noise on the “clean” supply. It is thus important that the additional noise on the relatively clean supply node does not exceed certain noise budget when transferring charge from the clean supply to the noisy supply. As the size of the inverter chain increases, its dynamic power also increases, at a benefit of the improved slew rate (SR). This effect can be shown in Fig. 5, where each buffer in the chain is sized up properly to produce the minimum path delay.

The current through the last stage of the chain $I_{last\_stage}$ determines the slew rate. The edge delay can be defined as the time for the positive plate of the decap to rise a full swing, as

$$\text{Edge Delay} = \frac{1}{SR} = \frac{C_{decap}}{I_{last\_stage}} \quad (1)$$

The edge delay is a better term in this scenario to illustrate the design tradeoffs in Fig. 5. Having an edge delay in the range of 50 to 100ps (i.e., 1/20 – 1/10 of a 1GHz clock period) is reasonable. Therefore, a buffer size of 300um/600um (NMOS/PMOS) for the last stage was selected to produce an edge delay of about 50ps, with a total dynamic power of around
3.8mW. Note that this dynamic power is not wasted, but rather transferred between the supply nodes. Only the power consumption of 65μW from the ring oscillator can be considered as power overhead, which is merely 0.2%.

When determining the size of the buffer chain, \( C_{\text{decap}} \) was chosen to be 700pF. Assuming a fixed edge delay, the size of buffer required is proportional to the decap value. If a smaller decap is used, the buffer size can be made smaller to dissipate less power. This power drawn from the clean supply node is critical so that the supply noise caused by the ring oscillator and the buffer chain should not rise beyond the noise budget in its localized region. That is, the goal of generating the “Clk” signal from a clean \( V_{\text{DD}} \) is to provide charge from the clean supply that is not connected to the main system clock or any important circuitry. The designer must ensure that the clean supply itself does not become excessively noisy so that the local supply integrity is compromised.

### C. Overall CBD Design

![Complete circuit diagram of charge-borrowing decap](image)

The complete charge-borrowing decap circuit is shown in Fig 6. An enable signal is provided to turn off the CBD for test purposes. When the enable signal is low, the transistor Msp is off, preventing current flow from the clean supply. The decap is implemented using PMOS transistors. When enabled, the voltage at B2 varies from 0 to 2\( V_{\text{DD}} \). The gate-source capacitance of Mdp1 creates additional noise on the clean supply node due to clock feedthrough. The existence of Msp provides shielding to the clock feedthrough to reduce this noise. The practical boosted voltage is 2\( V_{\text{DD}} \)-\( |V_{\text{thp2}}| \), while the charge provided per cycle is \( C_{\text{decap}} V_{\text{DD}} \). Note that the ESD concerns on the thin-oxide decap should be addressed by proper sizing of the two transistors, Mdp1 and Mdp2.

As described earlier, after a local hot spot is identified, the nearby passive decaps can be replaced by a CBD. Only the transistor Mdp2 needs to be implemented locally. Other circuits showing in Fig. 6 can be located away from the hot spot but near a clean supply node. The actual placement of the ring oscillator and the buffer chain will depend on the floorplan and location of power pins of the chip itself. Two global interconnects may be required to connect the two parts of circuits at node Clk and B1. Compared to the size of the passive decap, the size of Mdp2 is negligible, resulting in a very small area overhead in the local area.

### III. CHIP DESIGN AND EXPERIMENTAL RESULTS

To validate our design, a test chip was fabricated in a 1V-core STM 90nm process. The test chip setup and microphotograph are shown in Fig. 7 and 8, respectively. An active decap [4] of the same size was also implemented for comparison. For test purposes, the Clk signal was not generated from the ring oscillator, but from an external clock that was synchronized with the user logic clock.

![Complete circuit diagram of charge-borrowing decap](image)

In order to observe signals near the logic block, the supply variations were measured directly with probes. It is understood that the package inductance is an important source of power supply noise [8]. Since we did not use a packaged chip, two on-chip spiral inductors were implemented to mimic the package inductances, one on the supply path and the other on the return path. The value of the spiral inductors is close to a typical wire-bond package inductance.

The layout area for the passive decap, active decap, and CBD is about 0.6x0.15=0.09mm\(^2\) each. The total chip area is 1.1x0.86=0.95mm\(^2\). The decap circuits are placed about 0.6mm away from the user logic, in which a large buffer with a large capacitive load was used to create supply noise, with the input controlled by an external clock signal. The size of the passive decap was chosen to be only a few times larger than the capacitive load to create a ~100mV voltage drop for the experiments. The clock frequency was controlled externally using an Agilent 86130A analyzer. The probed pad of the supply node was connected to an Agilent DSO81304A oscilloscope to measure the voltage waveforms.

The average \( V_{\text{DD}} \) voltage per clock cycle is measured and compared since it is known to strongly influence the critical path delay of logical circuits [9][10]. A collection of 9 sample chips were tested. The improvement across the sample space is shown in Fig. 9, where the clock frequency was fixed at 27GHz.
1GHz for this test. The two sample chips that are in the fast process corner can be identified by correlating with simulation. In Fig. 9, the average supply voltage varies significantly mainly due to the random process variation on $R_{\text{mesh}}$ and $L_{\text{back}}$, which determines the IR drop on the supply rails. Note that the supply noise reduction improvement by using the CBD is rather consistent under process variations across dies, which indicates the robustness of the design. The sample chip that provides the best improvement was used for further analysis.

Fig. 9. Scatter plot comparing average $V_{\text{DD}}$ for the tested sample chips.

![Fig. 9. Scatter plot comparing average $V_{\text{DD}}$ for the tested sample chips.](image)

The waveforms of this test chip with a 1GHz clock are depicted in Fig. 10. The dark gray (blue in color) curve is when the CBD is on, and the light gray (red in color) curve is when the passive decap is on. The two curves are superimposed. Clearly, the supply voltage returns to high when extra charge is fed through from the clean supply on the rising edge of the clock, improving the average $V_{\text{DD}}$ level.

Fig. 10. Superimposed waveforms of a test chip on a 1GHz clock.

![Fig. 10. Superimposed waveforms of a test chip on a 1GHz clock.](image)

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REFERENCES


