



Product-Term Based Synthesizable Embedded Programmable Logic Cores

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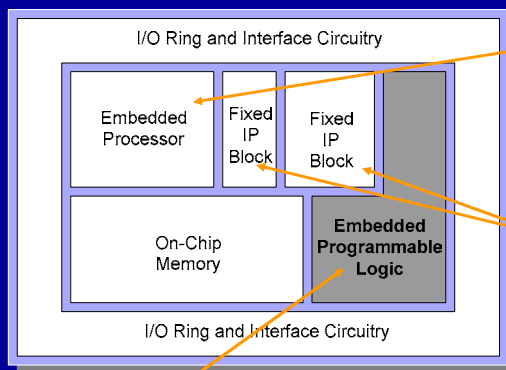
Overview of Contributions

- **Propose new architectural family for synthesizable programmable logic cores**
 - Basic logic element: Product-term array block
 - 35% density, 72% speed improvement compared to LUT-based architecture
- **Provide Sequential Circuit support**
- **Describe proof-of-concept chip employing novel architecture**

Background

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Programmable IP in SoC Design



Processor:

- Functionality specified using software

Fixed Logic:

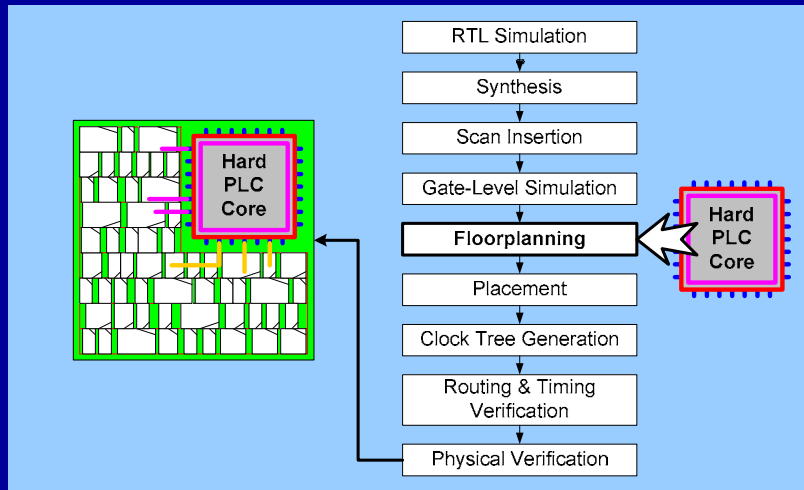
- Functionality fixed at design time
- Little post-fab flexibility

Embedded Programmable Logic:

- Functionality specified through hardware configuration

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“Hard” Programmable IP Flow



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Soft Programmable Logic Cores

- **Conventional approach**
 - “Hard” FPGA layout provided by vendors
- **Our approach**
 - Synthesizable Programmable Logic Core (PLC)
 - “Soft”: HDL used to describe a PLC architecture, NOT to describe a particular user circuit
 - Synthesis required to translate RTL to gates

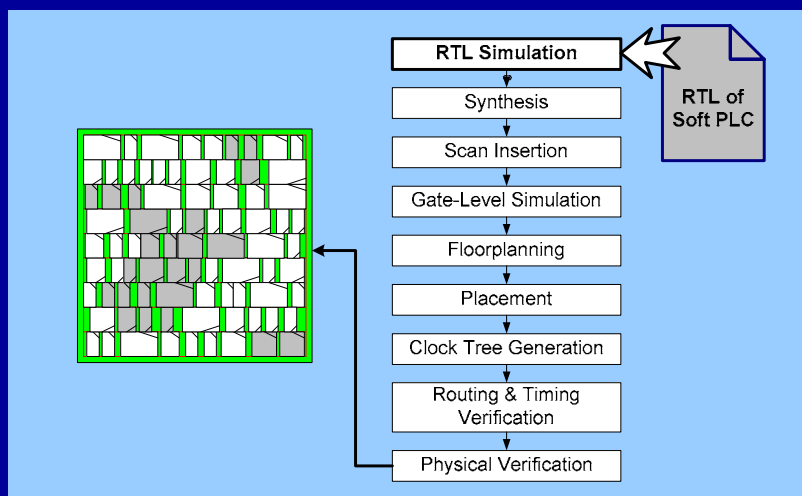
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Soft Programmable Logic Cores

- **Advantages**
 - Easy to integrate, reduces design time
 - Very flexible, can create the exact required core
 - Easy to migrate to smaller technologies
- **Disadvantages**
 - Inefficient compared to hard cores
- **Our thought**
 - Makes sense if you only want a small core (a few hundred gates, perhaps)
e.g. next state logic in state machine

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“Soft” Programmable IP Flow



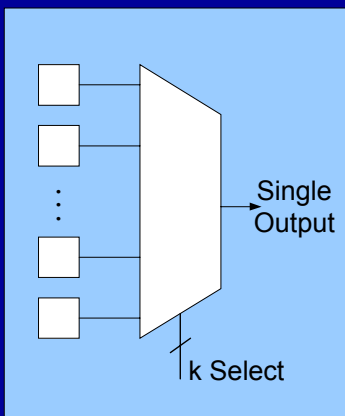
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Product-Term Block Synthesizable Architectures

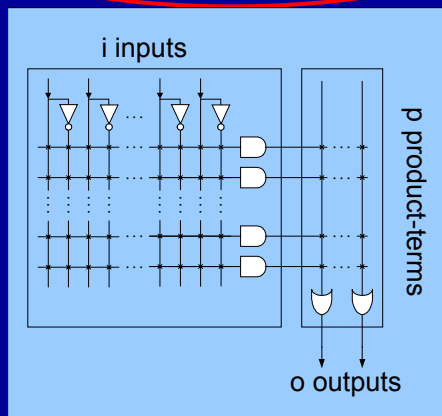
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Basic Logic Elements

Lookup-Table (LUT)



Product-term Block (PTB)



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Architectural Requirements

- **Area and delay minimization**
 - Large capacity product-term blocks (PTB) and shallow core depth
- **Simple placement and routing**
 - “Full connectivity” routing fabric
- **Flexible and scalable architecture**
 - Architecture parameter definitions and optimizations

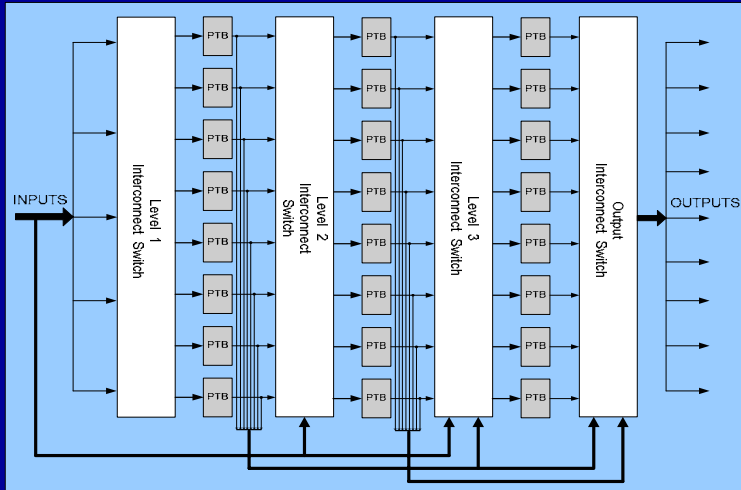
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Synthesizable PTB Architecture

- Product-term blocks (PTBs) arranged in several levels
- Unidirectional signal flow to avoid combinational loops in un-programmed fabric
- Outputs of PTBs in one level can only be connected to inputs in subsequent levels
- 2 interconnect strategies:
Rectangular and Triangular PTB architecture

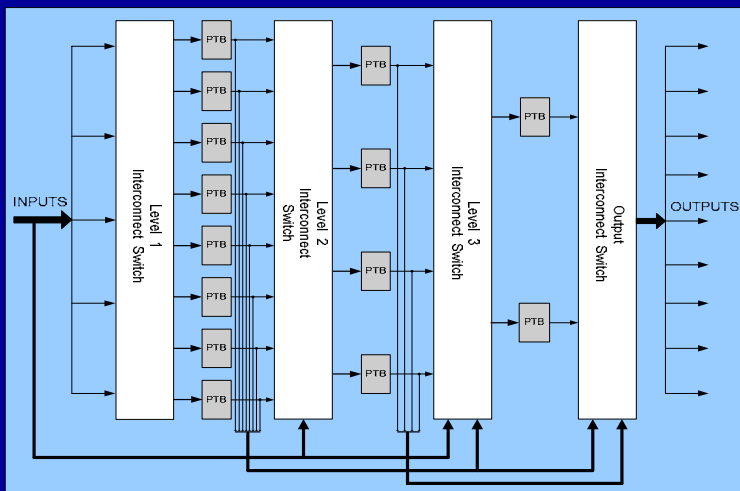
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Rectangular PTB Architecture



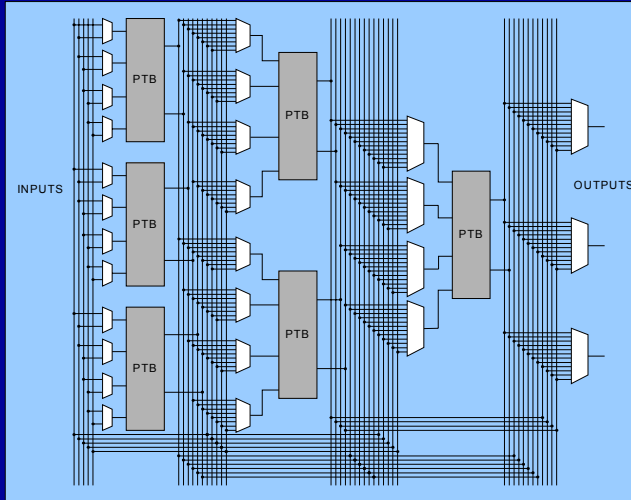
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Triangular PTB Architecture



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Detailed View of Interconnect Fabric

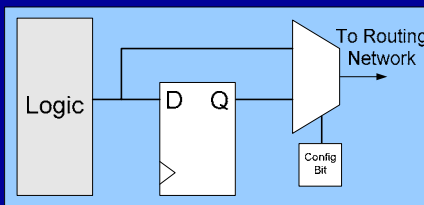


- Very flexible, not restrictive
- Easy P&R tools
- We can do better though

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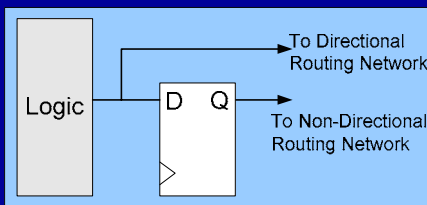
Sequential Circuit Support

FPGA-like Method:



- Multiplexer and flip-flop embedded into logic block to reduce stress on interconnect

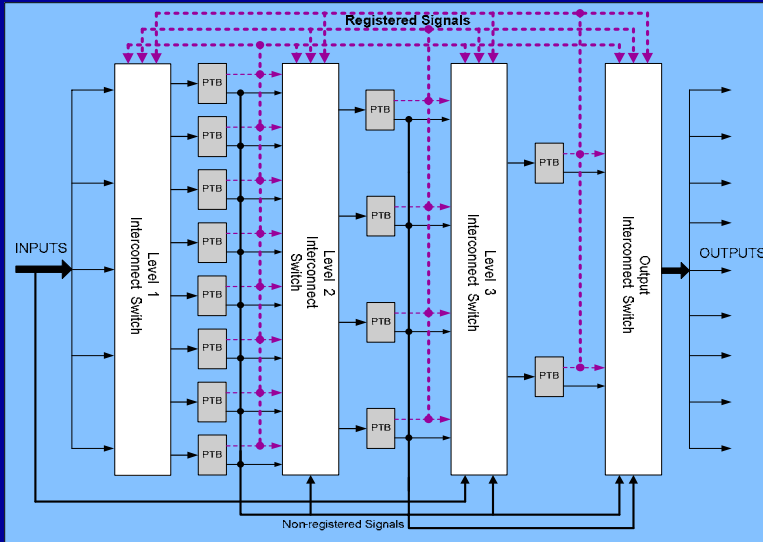
Synthesizable Method:



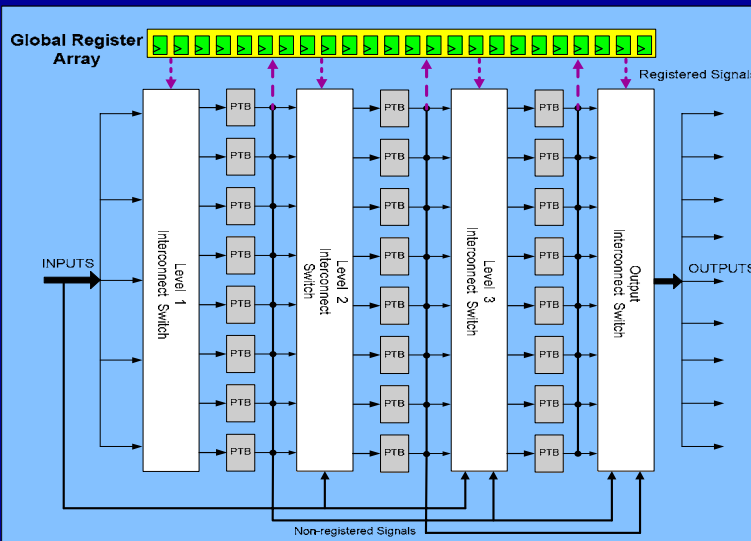
- Multiplexer removed to prevent loops in fabric
- Flip-flop may not necessarily be embedded into logic block

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Dual-Network Architecture



Decoupled Architecture



CAD Issues

- **Routing**
 - Simple, due to rich interconnect of PTB-based fabric
- **Placement**
 - Novel placement algorithm described in thesis
 - Employ greedy-based algorithm using slack analysis
 - Algorithm very close, or exactly same, to optimal results

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Parameter Optimization

Two Parameter Classes:

- **High-Level Parameters**
 - Specified by SoC core user / VLSI designer
 - Used to identify a specific core in a programmable library
- **Low-Level Parameters**
 - Not specified by SoC core user / VLSI designer
 - Used to describe specific characteristics of library
 - Determined through architectural experimentation

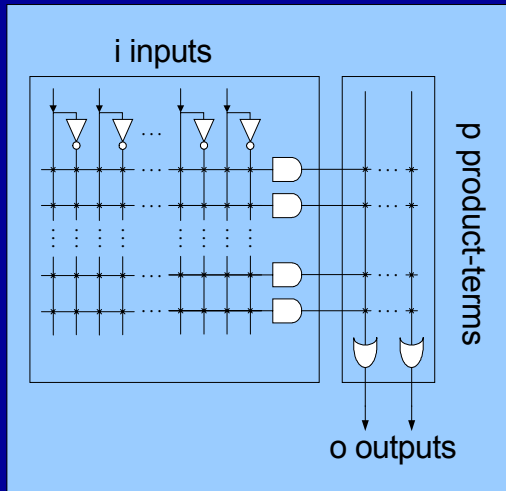
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Architectural Parameters

High-Level Parameters	Low-Level Parameters
Number of Primary Inputs Pins	PTB logic block: inputs (i), product-terms (p), outputs (o)
Number of Primary Output Pins	PTB interconnect structure: (r, α)
Number of Product-term blocks (PTBs)	Sequential interconnect: (v, d)

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Logic Block Parameter Optimization

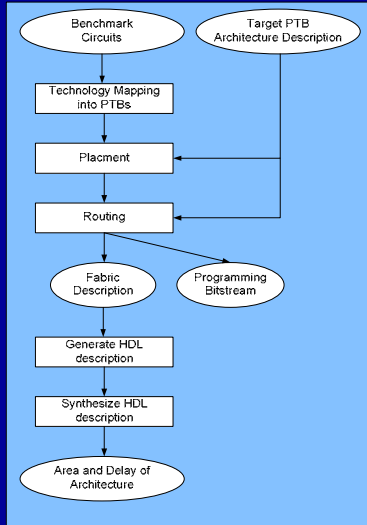


• 3 Product Term Block Parameters

- Number of Inputs, i
- Number of Product-terms, p
- Number of Outputs, o

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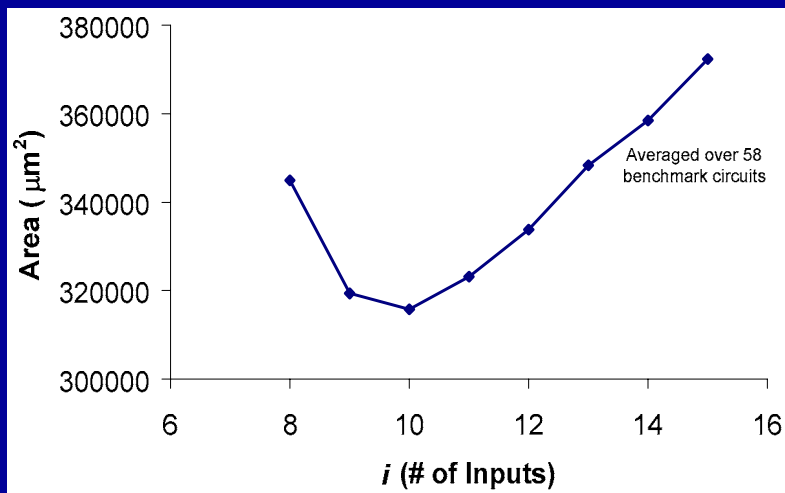
Experimental Methodology



- **105 MCNC benchmark circuits**
 - Ranging from 10 to 300 equivalent 4-LUTs
- **Technology mapped to PTBs using PLMap**
- **TSMC 180nm technology library**

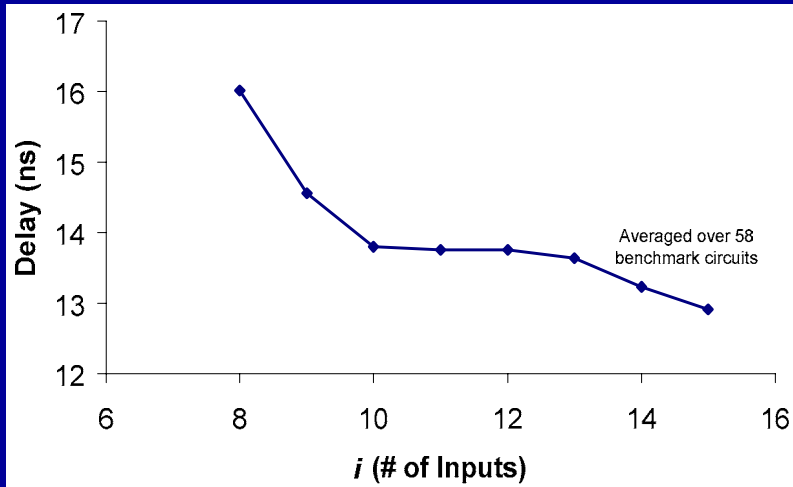
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Number of Inputs per PTB Area



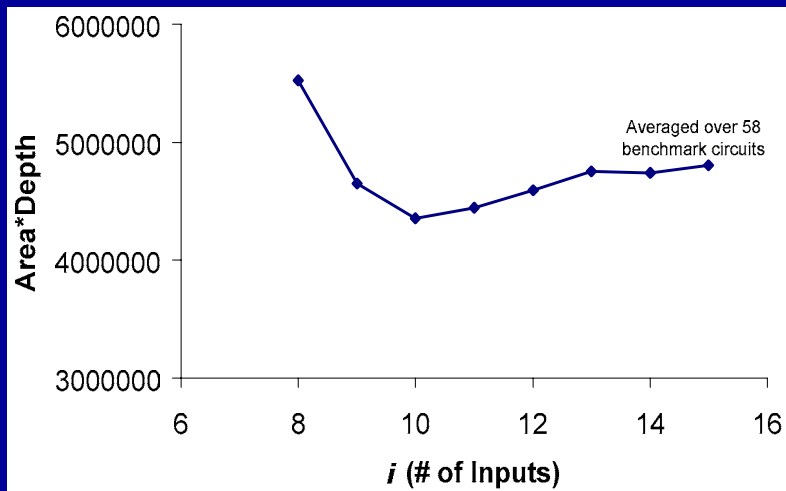
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Number of Inputs per PTB Delay



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Inputs per PTB Area*Delay



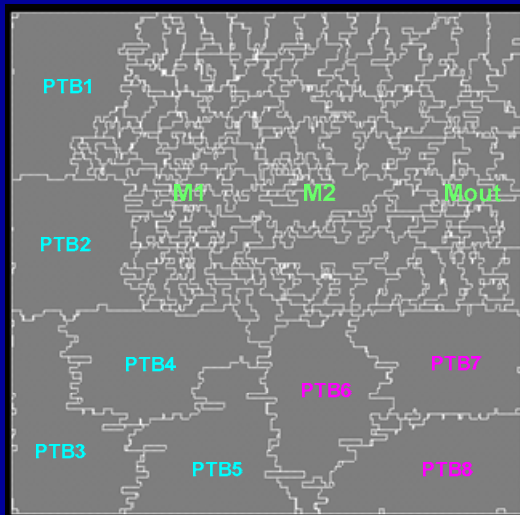
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Comparison to LUT-based Architecture

- 35% area improvement, 72% delay improvement
- Gains mainly from larger circuits (more than 50 equivalent 4-LUTs)
- Factors:
 - PTB-based architecture has larger and fewer logic blocks
 - PTB-based architecture routing fabric simpler and depth of core shallower

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Proof of Concept Implementation



- Automated placement closely matches conceptual view
- PTB 1-5: 1st level logic blocks
- PTB 6-8: 2nd level logic blocks
- M1, M2, Mout: interconnect blocks

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Comparison to LUT-based Architecture

	Product-Term Fabric	LUT-based Fabric
Area (μm^2)	238,000	396,000
Delay (ns)	5.5	10.0

- 12% area improvement, 40% delay improvement for this particular design

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Contributions

- Presented a product-term based synthesizable programmable logic device
- Presented two novel interconnect strategies
- Presented two methods to support sequential logic
- Developed place and route tools to support new architectures

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Contributions

- Optimized and investigated effects of various architectural parameters
- Described proof-of-concept chip
- Compared product-term architecture to lookup-table based device
 - Overall, 35% smaller and 72% faster
 - Primarily due to reduction in amount of circuitry needed to route signals

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References

- A. Yan, S.J.E. Wilton, "Sequential Synthesizable Embedded Programmable Logic Cores for System-on-Chip", in the *IEEE Custom Integrated Circuits Conference*, Orlando, FL, October 2004.
- A. Yan, S.J.E. Wilton, "Product Term Embedded Synthesizable Logic Cores", in the *IEEE International Conference on Field-Programmable Technology*, Tokyo, Japan, December 2003, Best paper award.
- A. Yan, R. Cheng, S.J.E. Wilton, "On the Sensitivity of FPGA Architectural Conclusions to the Experimental Assumptions, Tools, and Techniques", in the *ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*, Monterey, CA, Feb. 2002.

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