



An FPGA Architecture Supporting Dynamically Controlled Power Gating

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What this talk is about

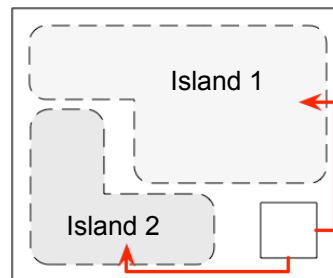
An FPGA Architecture supporting dynamic power gating:

- Turn off regions, at run-time, with on-chip control

ASIC designers do this regularly

Challenges for an FPGA:

- We don't know about application
- Routing for control signals
- Handling rush current in a programmable way





Motivation

High-end FPGAs are power-hungry

- Entering an era where we can't turn it all on at once!
- Need to selectively turn off regions when not being used
- Static control may not be enough...

Mobile hand-held applications

- Many applications have regions with long idle periods
- Could take advantage of this sort of architectural support

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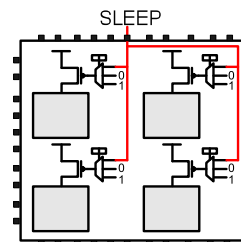
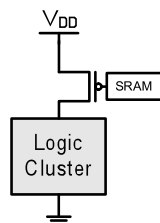
Relevant Work: Power Gating for FPGAs

Available FPGA power gating is **statically-controlled**

- Unused FPGA parts are turned off at configuration time

Some proposals exist for dynamic control

- Exploit DR to turn FPGA blocks on/off at runtime
- Sleep transistor could come from off-chip



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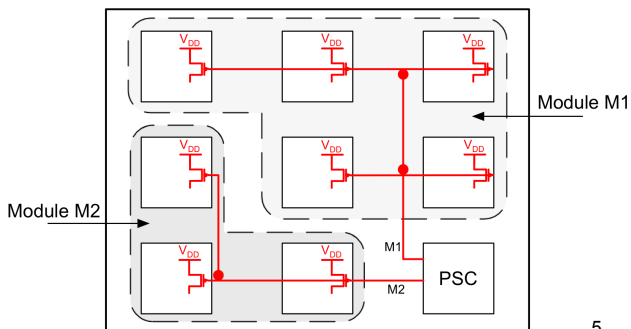
Our Architecture

Divide FPGA device into power-controlled regions.

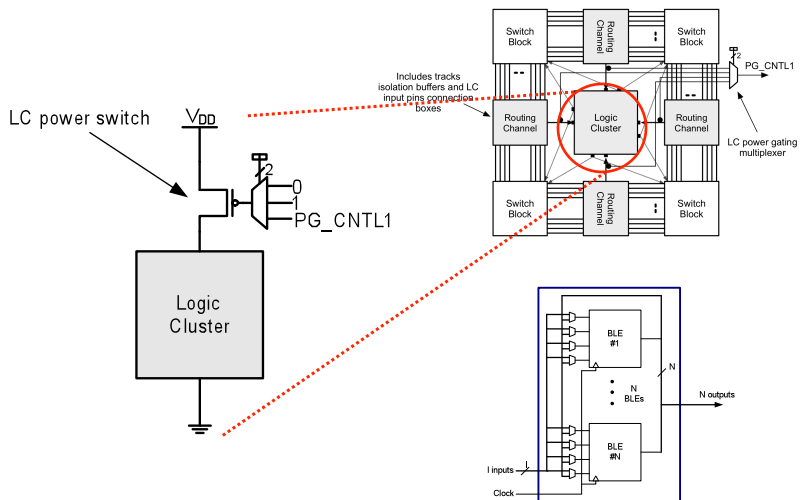
- Support dynamically-controlled sleep mode.

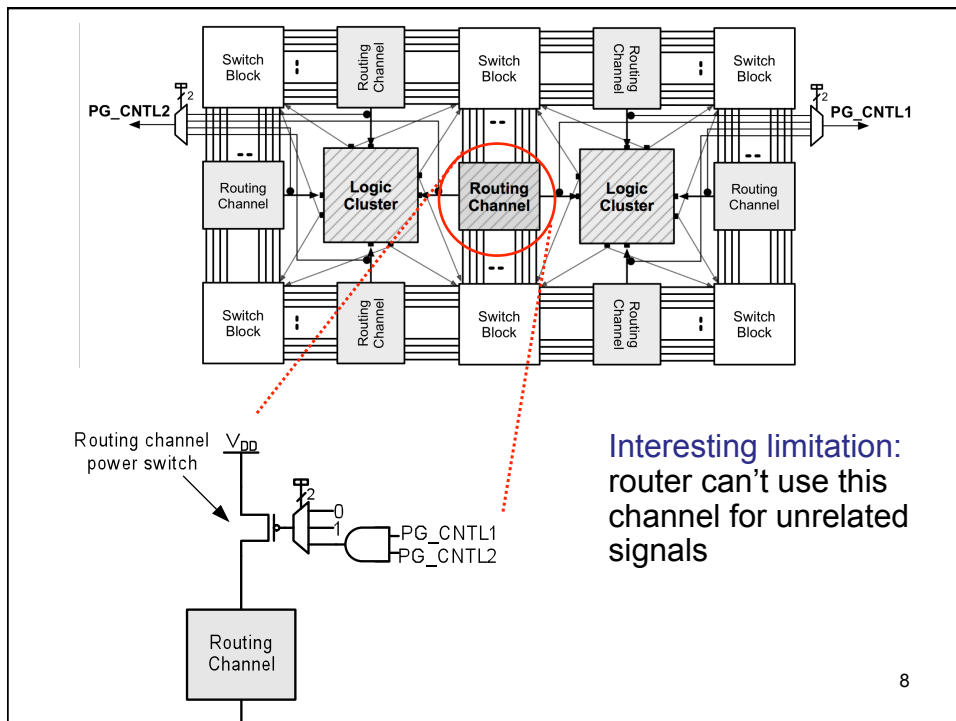
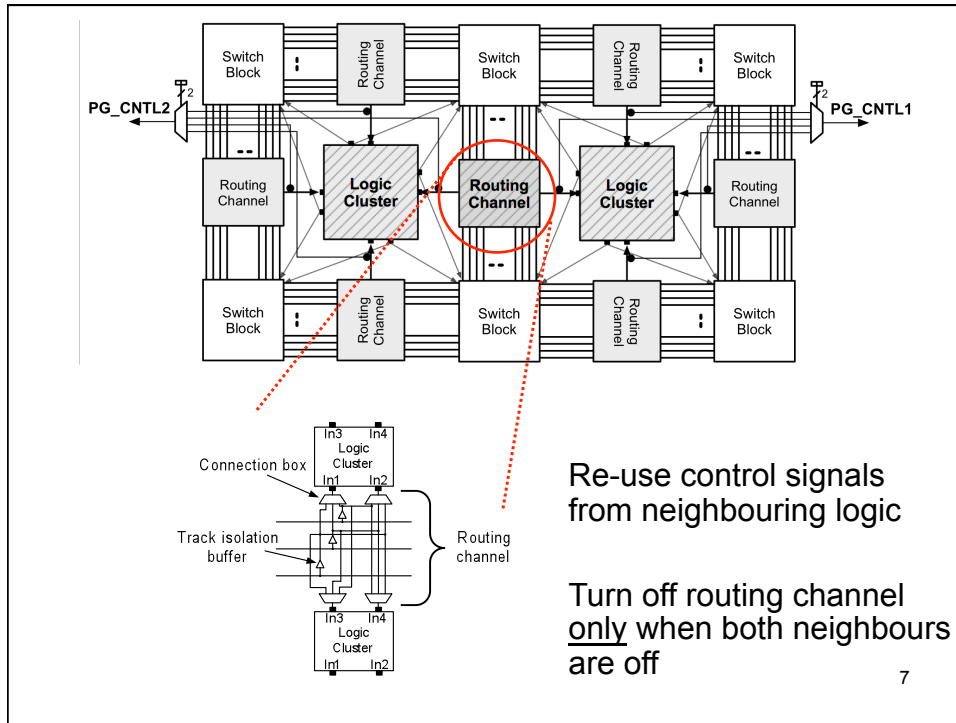
Use general-purpose routing fabric for control signals.

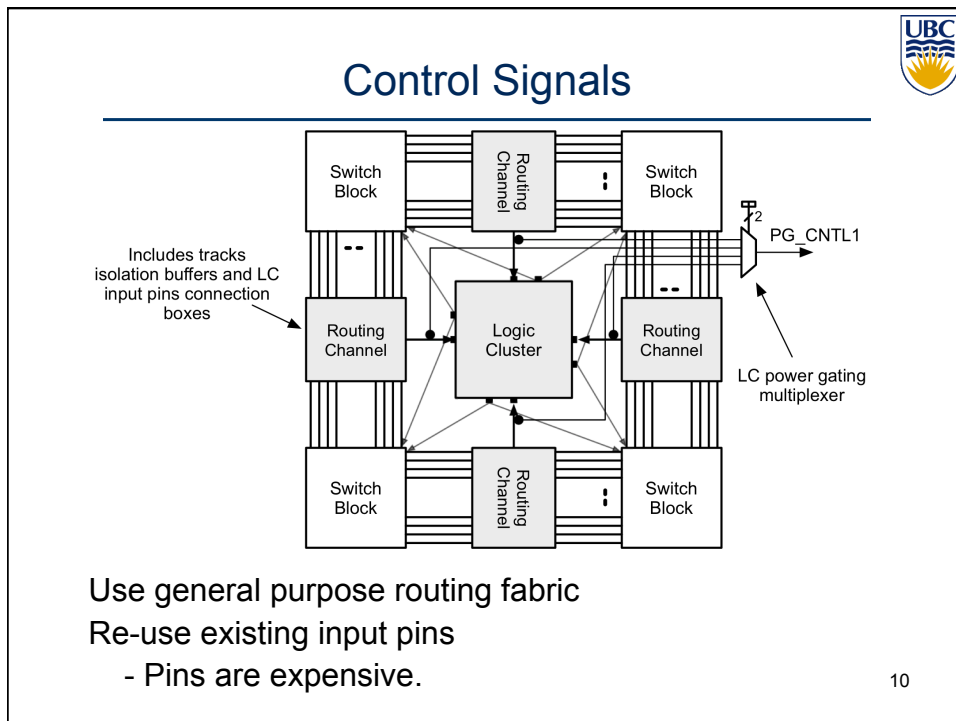
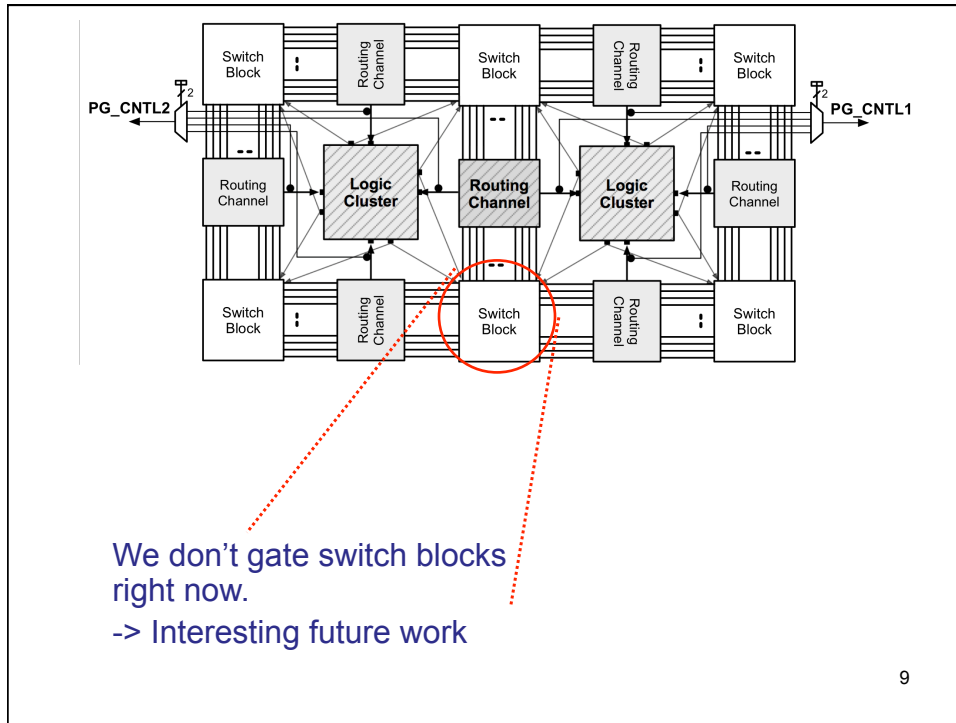
- Utilize unused input pins of logic clusters.



Basic PG Architecture – Logic Cluster







Area Overhead: Region Power Gating

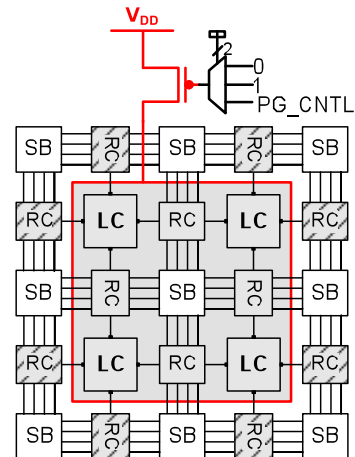


Can adjust granularity

- Share a sleep transistor among tiles

Interesting tradeoff:

area vs. "CAD difficulty"



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Rush Current



Problem: limit how much can be turned on at once

Possible solutions:

1. Expose it to the user
 - This is most familiar to an ASIC designer
2. Expose it to the CAD tool
3. Dedicated architectural support: programmable delay elements in turn-on circuits so they don't turn on all at once

Right now, we are doing #1

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Evaluation:

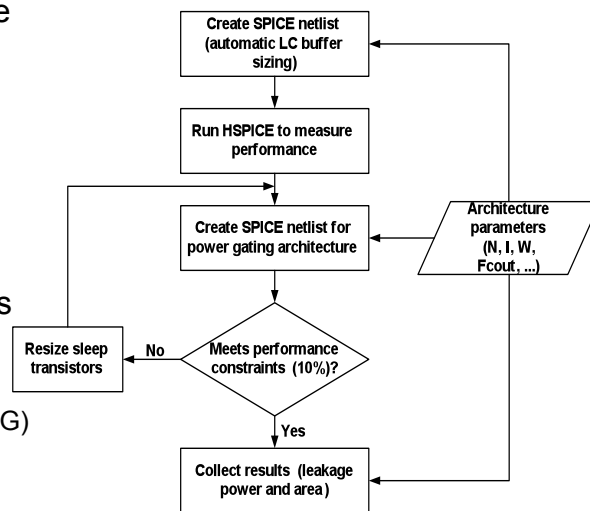
The Bad: Area, Delay, Leakage power overhead

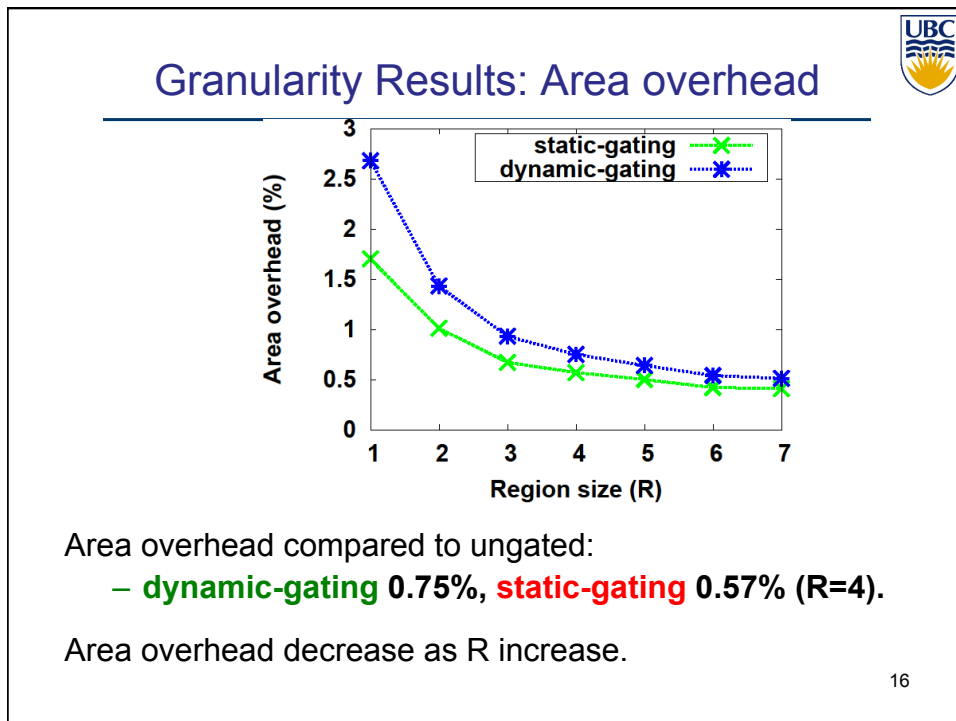
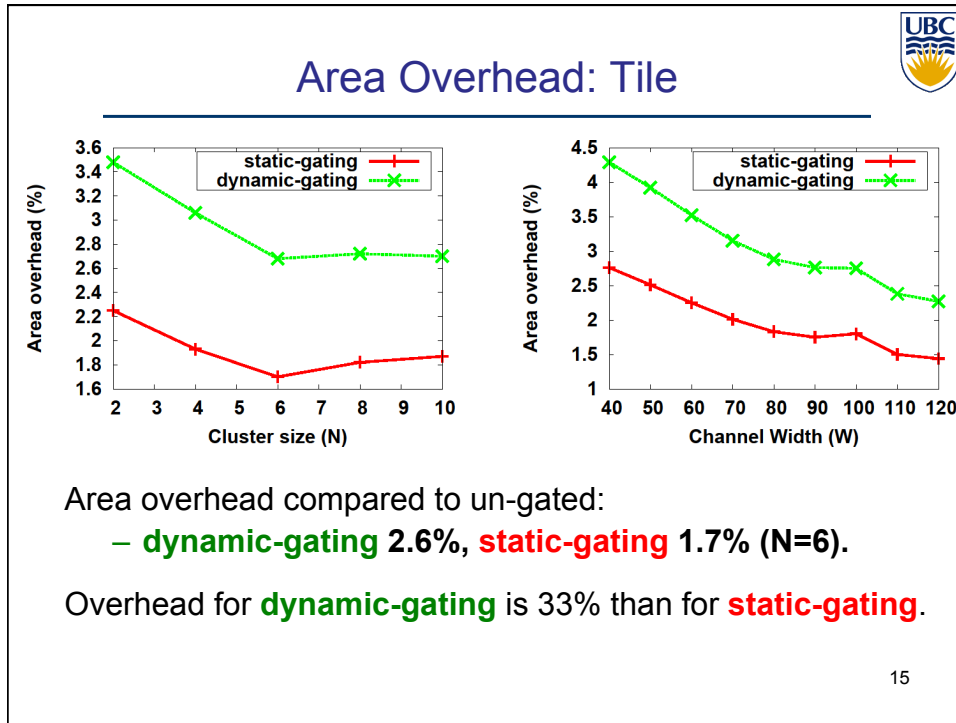
The Good: Potential leakage reduction

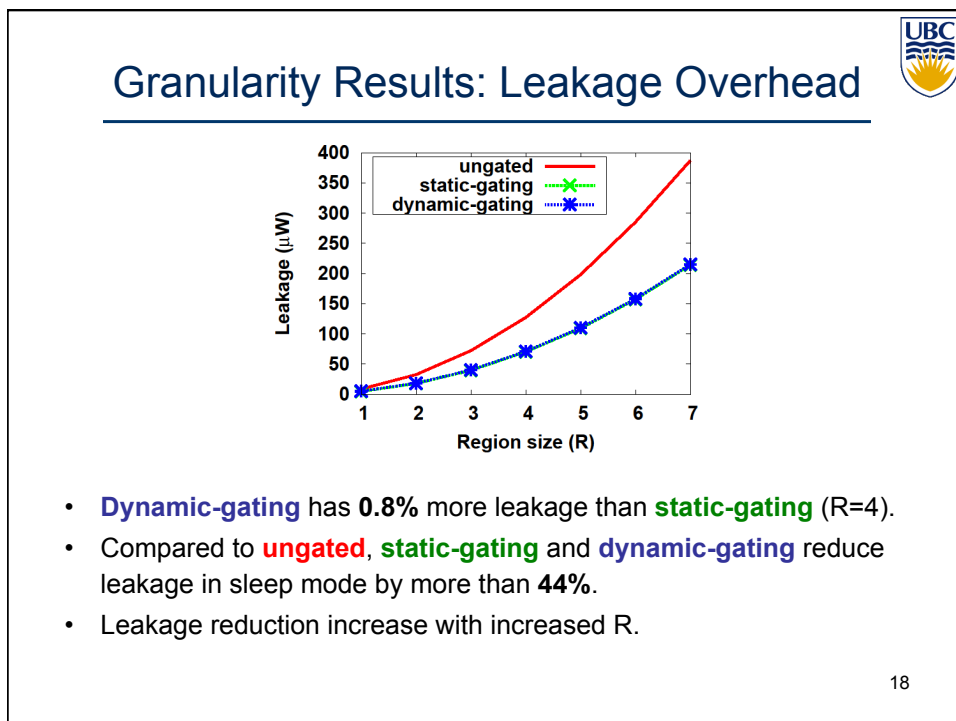
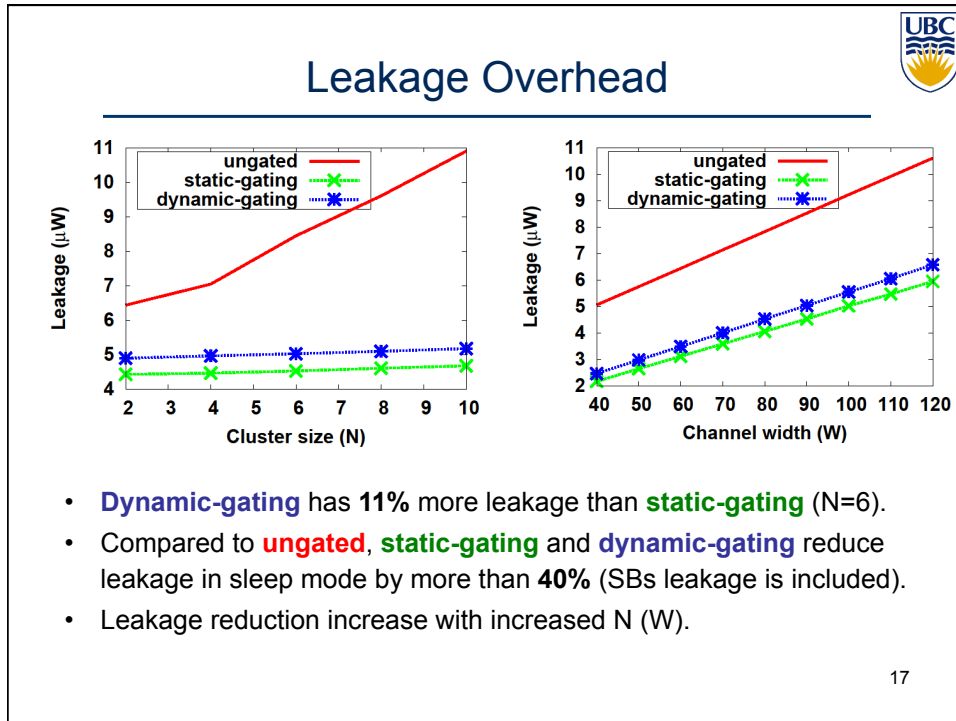
Experimental Setup



- Sweep architecture
 - N (cluster)
 - W (channel)
 - R (region)
- 45 nm PTM
- Three architectures
 - Ungated
 - Static-gating (SG)
 - Dynamic-gating (DG)







Delay overhead is 10% by design.

- We choose sleep transistors such that delay impact is no more than 10%
- Tradeoff: delay overhead vs. area overhead

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Potential Leakage Reduction



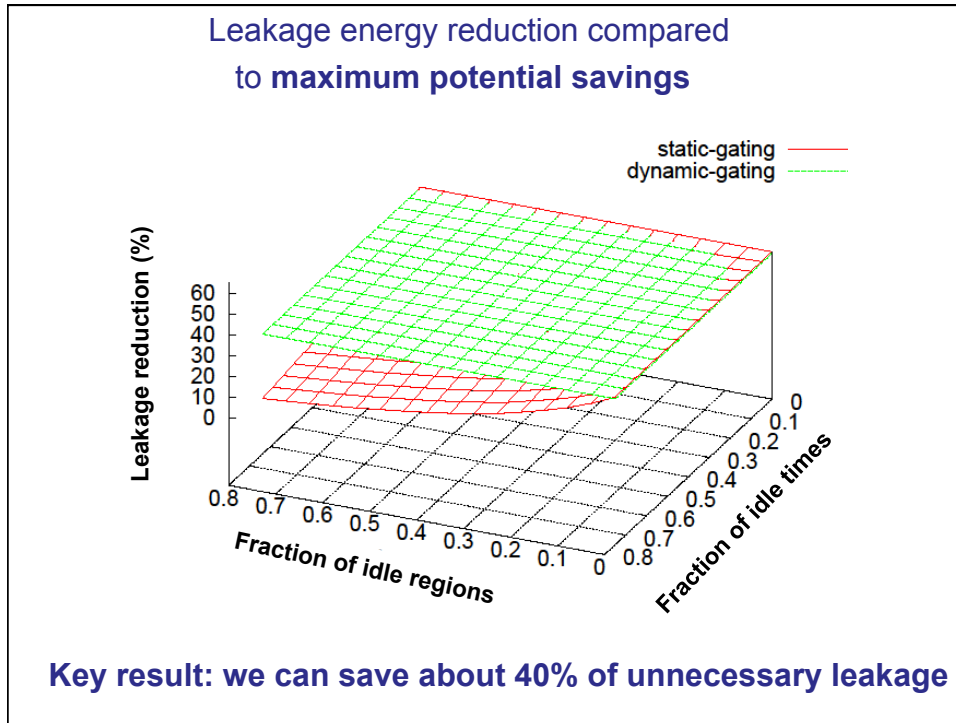
Use a model that relates:


- Number and size of idle regions
- Proportion of the time idle regions can be turned off
- Size of the “power state controller”
- Potential slowdown of application

... to the energy savings of the architecture

Goal: can we bound how much leakage we can expect to save?

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Summary

Dynamically controlled power gating is possible!

- can reduce 40% of unnecessary leakage
- Small area overhead, moderate delay overhead

Next steps:

- Need to turn off switch blocks
- This needs intelligent CAD tools
- Application mapping is tricky: how much can we automate?

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