

An Analytical Model Relating FPGA Architecture Parameters to Routability

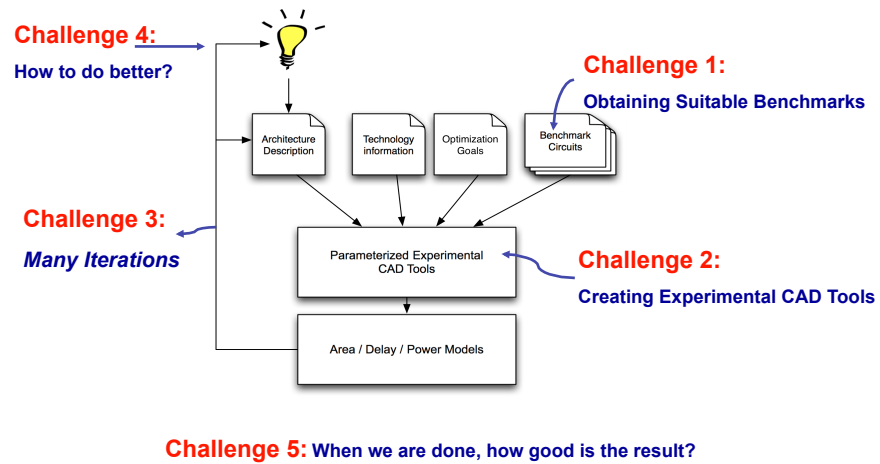


Joydip Das, Steve Wilton
University of British Columbia

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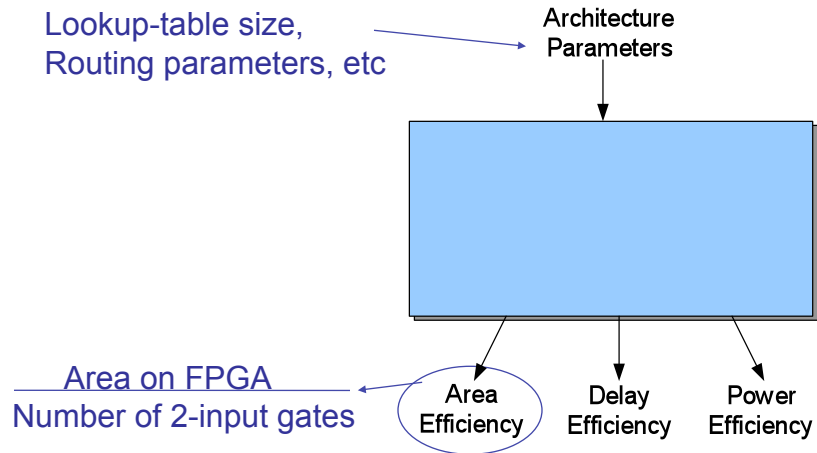
**Why do we need analytical model
for FPGA architecture design?**

Traditional *Experimental* Approach & Challenges

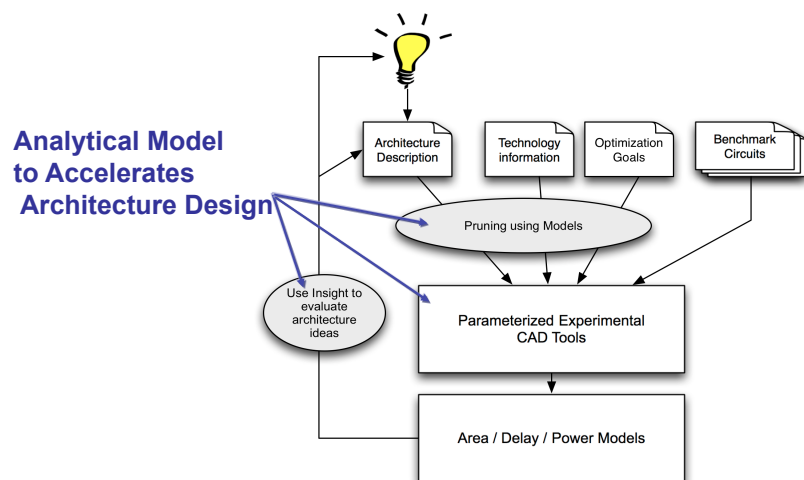


Can we supplement the experimental approach with analytical techniques?

Overview of Analytical Model

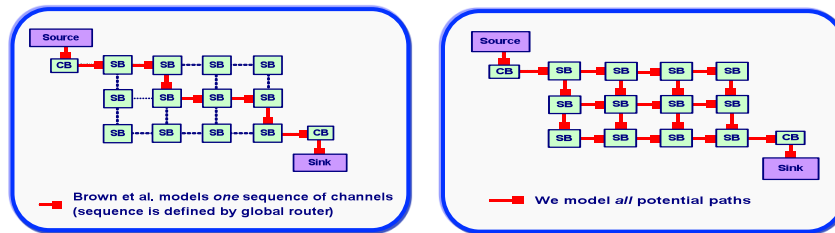


Accelerating FPGA Architecture Design



This Work:

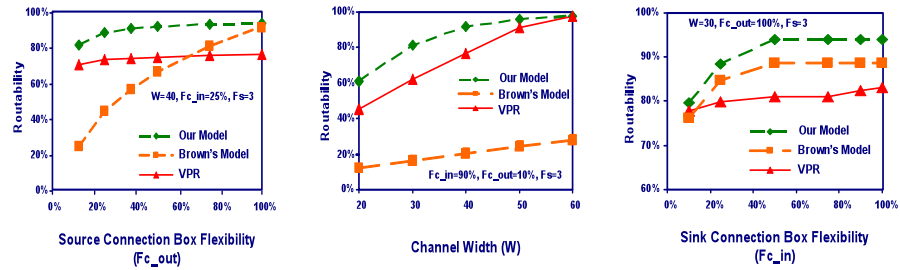
- We model the Routability as a function of Routing Fabric
- Very few works relate *Routability* to *Routing Parameters*:
 - Brown et al. [1992] models routability for detailed router
 - We model routability for global/detailed router [Pathfinder]
 - We use Brown's equations (with necessary modifications) and graph-theoretic techniques [Shantikumar '87, '88] to upper-bound the routability



This Work:

- Fast Routability Model will allow FPGA Architects to:
 - Investigate wide range of routing fabrics
 - Investigate area-delay trade-off in a timely manner

Validation Results



- **Our model follows the trends of VPR**
- **Our model overestimates VPR Results**

Summary

Key Result:

It is possible to model the routability for an FPGA global/
detailed router using analytical equations

This Talk:

- Presents such a model for Routability as a Function of Routing Fabric
- Presents the Validation Results