

Sensitivity of FPGA Power Evaluation

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Abstract

Power dissipation is becoming a major concern among FPGA vendors. Recently, architectural studies have been published which attempt to quantify the effects of various architectural alternatives on the power dissipation of FPGAs. These studies are very sensitive to assumptions made during the experimentation. In this paper, we analyze the sensitivity of two of these assumptions: the primary input density and the routing algorithm. We show that both of these assumptions significantly impact the architectural results.

1. Introduction

Power dissipation has become a critical issue for FPGA manufacturers. Understanding the power dissipation within FPGAs is the first step in developing power-efficient architectures and CAD tools for FPGAs. As presented in our previous research [3], a flexible power model has been integrated in the widely-used Versatile Place and Route (VPR) CAD tool, and it can be used to evaluate architectural tradeoffs and the efficiency of power-aware CAD tools.

Figure 1 shows the VPR framework with an activity estimator and a detailed power model for activity generation and power estimation respectively [3]. A transition density signal model [2][6] was applied to determine signal activities within the FPGA and calculate the dynamic power dissipation of the circuit. Short-circuit power is modeled to be proportional to the dynamic power dissipation. Leakage power is calculated using the basic model of SPICE for sub-threshold current. Also, an H-tree clock distribution network is employed in the model to model the power dissipated by the clock network.

Sensitivity analysis for FPGA research is crucial because experimental assumptions, tools, and techniques can significantly affect the conclusion of FPGA architectural experiments [5]. To investigate the sensitivity of power evaluation for FPGAs, we applied the flexible power model to perform experiments focusing on two sensitivity factors: the primary input transition density assumption and the routing algorithm.

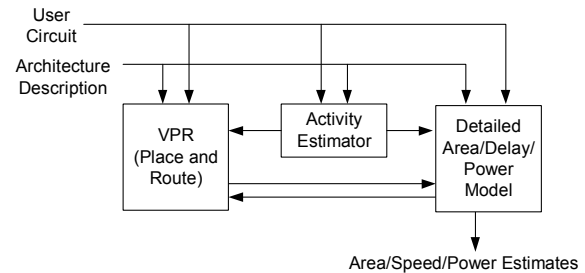


Figure 1 Modified VPR Framework

2. Sensitivity Analysis

Thirty-six circuits from the Microelectronics Center of North Carolina (MCNC) were used as benchmarks in our sensitivity experiments. Energy, instead of power, was used in our analysis to avoid bias by the clock frequency of the circuits. The following is our sensitivity analysis on the primary input transition density assumption and the routing algorithm.

2.1. Primary Input Transition Density Assumption

Because the switching characteristics of the primary inputs for the benchmark circuits are not available, researchers often model primary inputs as normalized random signals with a transition density value of 0.5; the signals are assumed to switch at 25% of the clock frequency. On the other hand, FPGA vendors suggest that typical switching rates of inputs range from 6% to 12% of the clock frequency; this corresponds to a transition density from 0.12 to 0.24 [4]. This discrepancy is important; the transition density values assumed for the primary inputs can have a significant impact on power evaluation. As shown in Figure 2, the energy consumed by the routing and the logic blocks increases when a higher value of primary input transition density is used. Note that the primary input transition density has more of an effect on the routing energy than the logic block energy because the routing wires contribute more capacitance than logic blocks. However, the primary input

transition density assumption does not affect the clock energy since the dedicated clock network is separate from the general-purpose routing.

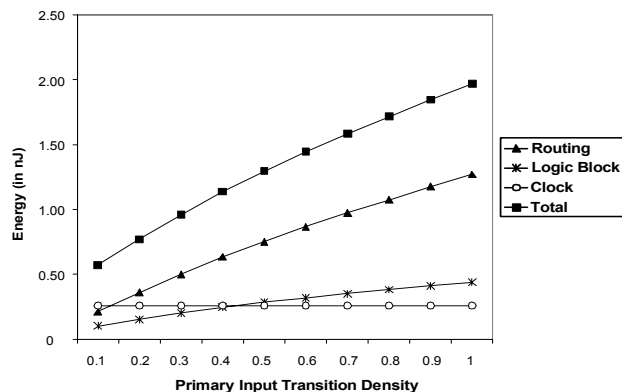


Figure 2 Energy versus primary input transition density

To further investigate the impacts of primary input transition assumption, we conducted two sets of experiments. The first set assumes primary inputs to be normalized random signal while the second set assumes that the primary inputs switch at a rate of 10% of the clock frequency (with a transition density value of 0.2) to reflect the statistical data from the FPGA vendors [4]. Our results show that the clock and leakage energy becomes more significant in the total energy consumption when a smaller value of transition density is applied to the primary inputs.

2.2. Routing Algorithms

VPR supports two routing algorithms: timing-driven and breath-first [1]. The timing-driven algorithm focuses on achieving a successful route by optimizing the circuit speed, while the breath-first algorithm emphasizes on routing a design by minimizing the number of routing tracks used [1]. According to our experimental results, the timing-driven algorithm yields circuits that consumed two times more power, but the average critical path delay of the circuits is 61% less than that using the breath-first algorithm. This is because the critical nets routed by timing-driven router use fewer tracks while the critical nets routed by the breath-first router have to be mapped to longer routes in order to reduce the number of tracks per channel in the FPGA. As a result, circuits obtained by timing-driven algorithm dissipated 22.2% less energy than those generated by the breath-first algorithm (see Figure 3). Our analysis shows that the timing-driven algorithm achieves more energy-efficient results on routing energy compared to the breath-first algorithm.

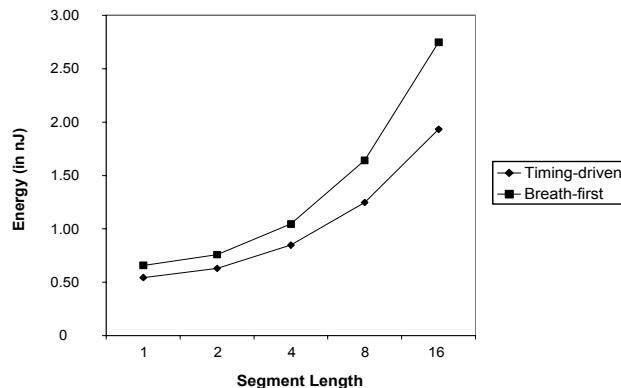


Figure 3 Routing energy using timing-driven and breath-first algorithms

3. Conclusions

Our sensitivity analysis shows that the results of our FPGA power estimation tool can be significantly affected by assumptions regarding the input transition density and the routing algorithm. Understanding these sensitivity implications is critical if the results of these experiments are used to guide the development of power-efficient FPGA architecture and CAD tools.

4. Acknowledgements

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References

- [1] V. Betz, VPR and T-VPack User's Manual, ver 4.30, March 2000.
- [2] F.N. Najm, "A Survey of Power Estimation Techniques in VLSI Circuits," IEEE Transactions on VLSI Systems, vol. 2, no. 4, December 1994, pp. 446-455.
- [3] K. Poon, A. Yan, S.J.E. Wilton, "A Flexible Power Model for FPGAs," in International Workshop on Field-Programmable Logic and Applications, September 2002.
- [4] Xilinx, Virtex Power Estimator User Guide, XAPP152, ver. 1.1, February 18, 2002.
- [5] A. Yan, R. Cheng, S.J.E. Wilton, "On the Sensitivity of FPGA Architectural Conclusions to Experimental Assumptions, Tools, and Techniques," in the proceeding of ACM International Symposium on Field-Programmable Gate Arrays, February 24-26, 2002, pp. 147-156.
- [6] G. Yeap, Practical Low Power Digital VLSI Design, Kluwer Academic Publishers, 1998.