An Analytical Model Relating FPGA Architecture Parameters to Routability

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ABSTRACT

We present an analytical model relating FPGA architectural parameters to the routability of the FPGA. The inputs to the model include the channel width and connection and switch block flexibilities, and the output is an estimate of the proportion of nets in a large circuit that can be expected to be routed on the FPGA. We assume that the circuit is routed to the FPGA using a single-step combined global/ detailed router. Together with the earlier works on analytical modeling, our model can be used to predict the routability without going through an expensive CAD flow. We show that the model correctly predicts routability trends.

Categories and Subject Descriptors

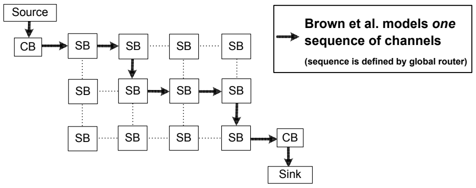
B.7.1 [**Types and Design Styles**]: Gate arrays

General Terms

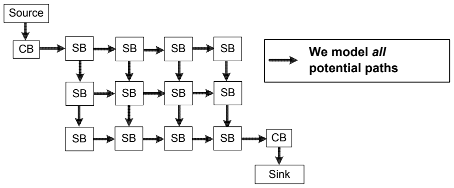
Design, Peformance, Measurement

Keywords

FPGA, Analytical Model, Architecture Development, Routability



a) Work of [3]: Routing of a net with length=6 for a detailed router



b) Our work: Routing of the same net for a single-stage combined router

Figure 1: The work of Brown et al. [3] and our work

1. INTRODUCTION

FPGA vendors invest significant resources in developing new logic, routing and embedded block architectures, and this activity shows no signs of diminishing. Traditionally, FPGA architectures have been designed and tuned using an experimental approach, in which designers perform numerous iterations of experiments, where benchmark circuits are mapped using representative computer-aided design (CAD) tools, and the effectiveness of potential architectures are validated using detailed area, power, and delay models [1, 2, 13]. Recent works have shown that this experimental approach can be supplemented by *analytical models* which relate the effectiveness of an FPGA to parameters describing the architecture of the FPGA [6, 7, 9, 10, 19, 18]. These models may accelerate the FPGA development process, allowing vendors to explore a much wider range of architectures, potentially leading to better devices. The models also provide important insight into what makes a good FPGA, and it has been suggested that they will be an important design tool for the rapid development of application-specific FPGAs [20].

A key part of any FPGA is the routing fabric. As new embedded blocks are added to an existing device, or as new logic blocks are designed, it is critical to ensure that the routing fabric provides sufficient routability and speed. Ensuring this can be helped by an analytical model that relates the overall routability of an FPGA to the architecture of that FPGA. Such a model would provide a fast way of estimating the routability impact of proposed architectural changes, allowing FPGA architects to focus only on potential architectures that are likely to be successful in routing the circuits.

Several techniques have been proposed to investigate the routability for FPGAs, such as, fGREP [11], RISA [4], Lou's method [12] and Rent's Rule Derivatives [17]. These works, however, do not relate routability directly to FPGA architecture parameters.

A model to predict the routability as a function of architecture parameters was described by Brown et al. [3]. However, that model makes the assumption that nets are routed using a two-stage *global/ detailed* router, as shown in Figure 1(a). With such a router, the set of channels that will be used by each net are determined using a global router, which does not consider the detailed routing architecture parameters. The detailed router then only considers routes that follow this sequence of channels. For example, in Figure 1(a), there are many potential paths connecting the source and the sink logic blocks. However, only *a single* set of channels will be selected by the global router and the detailed router will consider paths within these pre-selected channels. In Figure 1(a), the work of [3] mod-

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els the routability using only one such sequence of channels, such as the channels on the 'dark-solid' path, and will ignore the other potential channels, such as the 'light-dotted' paths.

In contrast, modern FPGA CAD suites usually employ a single-step *combined* global/detailed router [2]. Such a router considers all possible paths for each net, while simultaneously respecting the constraints imposed by the detailed routing architecture. Thus, we would expect that the routability predicted by the model in [3] may be quite different than that experienced by the modern routers. We present results that show that this is indeed the case. Our results further show that, for a combined router, the model of [3] can not properly capture the trend of the changes in routability values with respect to the changes in routing architecture.

We present a routability model that better captures the behavior of a modern FPGA combined router. Our model considers all potential paths between the source and the sink nodes, as shown by the 'dark-solid' lines in Figure 1(b). The model contains a set of simple closed-form expressions that relate the FPGA architectural parameters to routability. More specifically, the output of our model is an estimate of the routability of the routing fabric, in terms of *the expected proportion of the nets in a large circuit that can be successfully routed*. The inputs to our model are the FPGA architectural parameters: channel width W; connection block flexibilities $F_{c_{in}}$ and $F_{c_{out}}$; and switch box flexibility F_s. The input parameters also include a small number of circuit parameters (minimum grid-size to implement a circuit N_{xy}, total number of nets $|\Psi|$, post-placement average wirelength l_{avg} and post-placement maximum wirelength l_{max}). The circuit dependent input parameters can be obtained from the earlier works on analytical modeling [6, 14, 19]. Combined with these earlier works, our model can predict routability without going through the expensive stages of a CAD flow.

We observe that our problem is related to the problem of estimating the reliability of a stochastic network with given network constraints. Numerous publications have attempted to determine the reliability of a connection between the source terminal and the sink terminal of such stochastic networks [5, 8, 16, 15]. Out of these works, Shanthikumar uses the consecutive minimal cutsets of a stochastic network for bounding the reliability of systems [15, 16]. We apply the techniques from Shanthikumar to our problem.

We show that our model can successfully predict the routability for a combined router. We also show that our model performs better than the previous model [3] when a combined router is used. We further demonstrate that our model can correctly predict the routability trends with respect to the changes in the routing architecture. The latter suggests that our model will be a valuable tool for FPGA architects in the early stage architecture evaluation.

The rest of the paper is organized as follows. Section 2 presents the model formulation. Section 3 validates our model and explains the results. Finally, conclusions are presented in Section 4.

2. MODEL FORMULATION

In our derivation, we make two important simplifications. First, we assume that each net has only one sink. As we will later show, even with this simplification, we get acceptable results. The second simplification is that all nets are routed using their shortest path.

The formulation of our model consists of three stages, as briefly described below. Due to space, we do not present the equations that we derive in each stage, however an implementation of the model can be downloaded from *http://www.ece.ubc.ca/~dasj*.

2.1 Stage I: Formation of the Graph

Stage I of the model formulation consists of two phases. First, we assume the use of a combined router and construct a graph $G(V, E)$ to represent the possible routing paths *for a single net with a given length*. Each vertex V represents a switch box (SB) or a connection box (CB) along the path of this net. A directed edge E represents a channel connecting two vertexes.

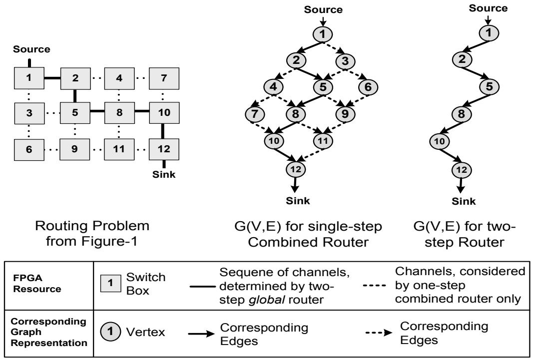


Figure 2: Graph G(V,E) for the routing problem in Figure 1

For the example routing problem of Figure 1, Figure 2 shows the graph $G(V, E)$. We omit the CB nodes for clarity. For completeness, we also show the graph $G(V, E)$ that would be obtained if a two-step detailed router was employed.

After forming the graph $G(V, E)$, we assign weights to the edges of $G(V, E)$. The weight of an edge (channel) corresponds to the routability of the net across this channel, as a function of FPGA architectural parameters. This weight depends on the distance of the channel from the source node (CB) along the path of the corresponding net. Brown et al. [3] models the probability of successful routing across the SBs along the path of a net with given length. We use this model to assign weight to a channel. We make necessary modifications to the equations of [3] to make them more suitable for the later stages of our model.

Without loss of generality, as shown in Figure 2, we assume that all connections enter a SB from left or top, and exit the SB from right or bottom. In our model, we divide the SBs into two types. All SBs on the top and the left side of the grid will be referred as *Type 1* SBs, and the other SBs will be referred to as *Type 2* SBs. Type 1 SBs have the property that if they are used in the path of the net, the net will only enter this SB from one side. On the other hand, the Type 2 SBs have the property that the net may enter from one of *two* sides. Our weight assignment differentiates between these two types. In Figure 2, example nodes for Type 1 SBs are 1, 2, 3; and example nodes for Type 2 SBs are 5, 8 and 9.

We make an important approximation in assigning weights to the *Type 2* SBs. We assume that if a tracks are incident from either side, they will combinedly attempt to connect to $max(2a, W)$ number of tracks on the outgoing side. In other words, two sets of incident tracks will connect to separate sets of outgoing tracks. This may not be the case since some incident tracks from the horizontal and the vertical directions may be connected to the same outgoing track of the SB. Thus, our model may provide optimistic values for routability. The other approximation that we make is that the conditional events of success for the channels incident to a SB are independent. The relaxation of these approximations may be an interesting topic for future research.

The output of stage I is the graph $G(V, E)$ that captures all possible paths for a net in a combined router; and the weigths associated with the edges. Our work can be extended to remove the shortest path constraints. Compared to the $G(V, E)$ for shortest-path routing, the extended graph will have more vertices and edges.

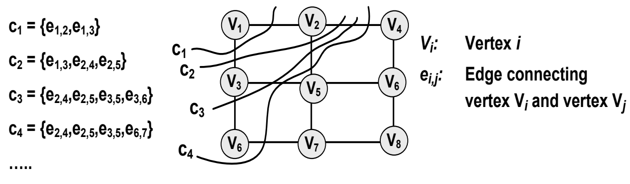


Figure 3: Examples of consecutive cutsets

2.2 Stage II: Overall Routability of a Net

The next step is to use the graph $G(V, E)$ from Stage I to estimate the overall routability of one net in the circuit with a given length. In doing so, we model the routability of the net on a *two-dimensional* grid. We are interested in computing the probability that *at least one* potential path is available to route the net.

We use methods from network reliability theory. Several studies in the reliability domain consider methods to bound (upper and/or lower) the reliability of a multipath network. These studies perform this task by finding the probability of having at least one successful path between the source terminal and the sink terminal, given the failure rate of each link [5, 8, 15]. Our problem is similar, we consider a "failed link" along a potential routing path to consist of at least one channel that is too congested to route the net.

We use the technique proposed by Shanthikumar [16, 15] to bound the routability of a net with given length. Shantikumar uses the consecutive cutsets to *upper*-bound the reliability of a network. To use this technique, we first determine the ordered set of r number of consecutive minimal cutsets C, where $C \equiv c_1, c_2, \cdots, c_r$. In Figure 3, we present example consecutive cutsets for a graph. A net is unroutable only when all the edges (FPGA channels) on at least one consecutive minimal cutset fail. For example, the net in Figure 3 will be unroutable if each of the edges of the cutset c_2 (such as, $e_{1,3}$, $e_{2,4}$ and $e_{2,5}$) fails.

We use the edge-weights from Stage I to model the probability of such failure events. This consequently gives us the probability of successful routing of a single net with given wirelength, while considering all possible routing paths between the source terminal and the sink terminal. For the Ψ_i th net with length l, we denote this probability as $Pr[R_{\Psi_i|l}]$. Due to space, we omit the detailed analysis and the mathematical expressions related to this stage.

2.3 Stage III: Routability of a Net with Any Probable Length

We next model the routability of a single net that may assume any length within the range (1, l_{max}) with l_{max} being the maximum wirelength. Assuming the geometric wirelength distribution [3], we express the routability of a net Ψ_i by:

$$Pr[R_{\Psi_i}] = \sum_{l=0}^{l_{max}} Pr[\Psi_i|l] \cdot Pr[R_{\Psi_i|l}] \tag{1}$$

where, $Pr[\Psi_i|l]$=$p_\Psi \cdot q_\Psi^{l-1}$, with p_Ψ=$1/l_{avg}$ and q_Ψ=$1 - p_\Psi$. l_{avg} is the average wirelength of two-terminal nets for the circuit being modeled. We can substitue $Pr[R_{\Psi_i|l}]$ from Stage II to determine the routability of a net, that does not have any length constraint.

We find that, due to the geometric nature of the wirelength distribution, the probability term $Pr[\Psi_i|l]$ in Equation 1 diminishes with the increasing value of length l. In other words, ignoring the higher values of l in Equation 1 will only weakly affect the overall routability of the net. This observation allows designers to use a lower value of l_{max} to speed up the estimation process.

Finally, the routability of a circuit with total $|\Psi|$ number of two-terminal nets (Ψ_i's) can be expressed by the following equation:

$$Pr[R_{ckt|comb}] = \frac{1}{|\Psi|} \cdot \sum_{i=1}^{|\Psi|} Pr[R_{\Psi_i}] \tag{2}$$

3. MODEL VALIDATION

In this section, we compare our model predictions with experimental results, obtained using VPR [2]. We also compare our predictions with the predictions from the model by Brown et al. [3]. We investigate the effects of varying routing architecture parameters, such as W, $F_{c_{in}}$, $F_{c_{out}}$ and F_s.

3.1 Methodology for collecting model results

To model the routability of a circuit, our equations require the grid-size needed to implement the circuit N_{xy}, the average post-placement wirelength l_{avg}, and the maximum post-placement wirelength l_{max}. These parameters are modeled using earlier works. N_{xy} can be approximated as $\sqrt{n_c}$, where the number of clusters n_c is obtained from the model in [6]. Similarly, l_{avg} and l_{max} can be modeled respectively from the works in [19] and [14]. We use these input parameters in our model and find the routability values by sweeping the routing architecture parameters. To obtain the results for the earlier model [3], we directly use their equations.

3.2 Methodology for collecting VPR results

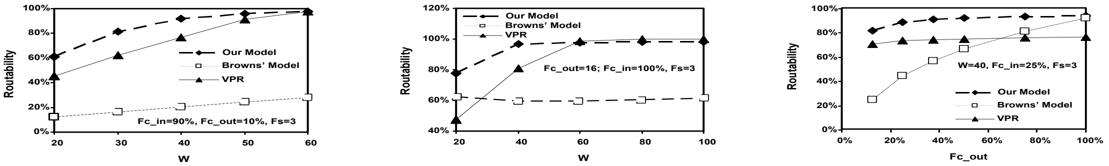
We first attempt to route a circuit in VPR using 50 iterations [2]. We approximate the minimum-path constraint by setting the *bb* flag to 0. If after 50 iterations, some nets can not be routed, we break down the multi-terminal nets into two-terminal nets. We then iterate through these two-terminal nets to investigate the resources that they use. For a net, if the capacity of any used resource is lower than the occupancy of the same resource, we mark the corresponding net as unroutable. For all resources that this net uses, we decrement the occupancy values by one. After iterating through all two-terminal nets, we calculate the percentage of the nets that are routable for the corresponding set of architectural parameters.

3.3 Validation Results

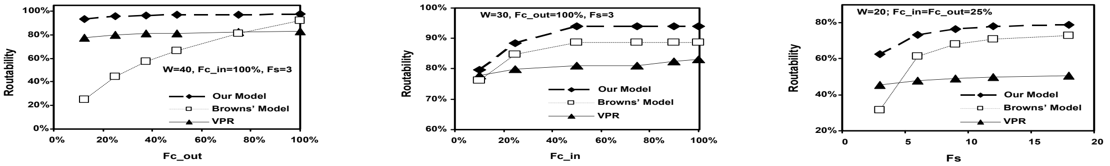
Figure 4 presents the results. As we can see from the Figure 4, our model is more accurate than the earlier model of [3] in most cases, especially for the highly constrained architectures. We also find that the earlier model can not properly capture the trend of the experimental results with respect to the changes in routing architecture. Thus, when a combined router is used, the designers can not use this model to investigate the effects of routing architecture parameters on routability. These observations justify the extension that we present in this paper for a combined router.

We find that our model predictions follow the routability trends with respect to the architectural parameters quite closely. We believe that this characteristic makes our model a valuable tool in modeling routability in the early stage architecture evaluation.

From Figure 4, it is clear that our model overestimates the experimental results, especially for the resource constrained architectures. From our earlier discussion, we identify three reasons for such over-estimation. First, since we use the upper bounds of the routing graph $G(V, E)$ to estimate the routability, the model is expected to over-estimate the experimental results. Secondly, we assume that the switch box construction is such that two sets of incident tracks will connect to the separate sets of tracks on the outgoing side of the switch block. Finally, the methodology that we follow in collecting experimental results contributes to the over-estimation of the model results.



(a) Validation for channel-width W (b) Validation for channel-width W (c) Validation for $F_{c_{out}}$



(d) Validation for $F_{c_{out}}$ (e) Validation for $F_{c_{in}}$ (f) Validation for F_s

Figure 4: Validation for 10 MCNC benchmark circuits (geometric average)

4. CONCLUSIONS

In this paper, we have presented an analytical model relating FPGA architectural parameters to the routability of an FPGA. We assume that the circuit is routed on an FPGA using a single-step combined global/detailed router. Through comparisons to VPR, we have shown that the model correctly predicts routability trends.

We envisage that this model will be useful during early stage architecture investigation, when architectures are being evaluated without the luxury of having a complete experimental CAD flow. We believe that in combination with previously published models [7, 14, 19], our model can provide useful insight into routability during these early stages of architecture investigation, allowing FPGA architects to quickly rule out "bad" architectures, and identify "interesting" architectures for more detailed evaluation.

There are a number of limitations to our model. First, we consider two-terminal nets for modeling routability. Second, we approximate a switch box construction in which we assumed that incoming tracks from different directions can connect to separate set of outgoing tracks. We also assumed that the events describing the number of available tracks to each channel incident to a switch block are statistically independent. Future work should address each of these limitations, and evaluate how much of an impact they have on the overall accuracy of the model. Follow up work may also target the improvement of CAD tools utilizing the routability information, obtained from this work. An executable version of our model can be downloaded from *http://www.ece.ubc.ca/~dasj*.

5. ACKNOWLEDGMENTS

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