

Charge-Borrowing Decap: A Novel Circuit for Removal of Local Supply Noise Violations

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Abstract- We propose a novel circuit called charge-borrowing decap (CBD) as a drop-in replacement for passive decaps to reduce supply noise for removal of “hot-spot” IR-drop problems found late in the design process. Measurement results on a 90nm test chip show that a noise reduction improvement between 42%-55% at 100MHz-1.5GHz over its passive counterpart.

I. INTRODUCTION

The increase in clock frequency and on-chip current demand makes power grid design a challenging task. Decoupling capacitors (decaps) are generally used to reduce IR drop and Ldi/dt effects, and hence keep the power supply relatively constant. Starting from 90nm, simply placing passive decaps in the available open areas of the chip may not be sufficient [1]. Large power supply noise levels in localized regions (called “hot spot” IR-drop violations) may unexpectedly be present in high-speed applications. These unresolved hot spots cause timing closure problems or result in functional failures in extreme cases. To remove them, active decaps [2][3][4] have been proposed for use as a drop-in replacement of the passive decaps. The use of active decaps saves time and effort near the tapeout deadline, and therefore provides an attractive solution. This paper proposes a novel charge-borrowing decap (CBD). The CBD design provides significantly more charge than a passive decap to reduce the local supply noise level, with only a minimum power loss during charge transfer from a clean supply node. As a result, the new circuit provides better noise reduction performance than passive decaps and even active decaps. With a relatively simple and robust design, the CBD only requires a small area overhead.

II. CHARGE-BORROWING DECAP CONCEPT AND DESIGN

A. Charge-Borrowing Decap Concept

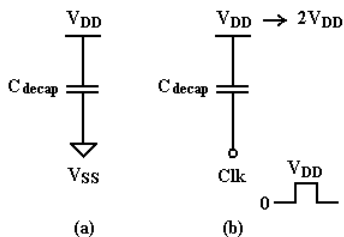


Fig. 1. CBD concept shown in (b), compared to a passive decap in (a).

The main purpose of a decap is to provide charge to stabilize the supply voltage locally. Unlike a passive decap, which provides charge from itself, our new circuit “borrows” charge from a clean supply node to reduce local noise level. This charge borrowing is accomplished using the effect of capacitive feedthrough, as illustrated in Fig. 1. For a fixed

decoupling capacitance of C_{decap} , we assume certain supply noise kV_{DD} is present on the supply, where k is a fractional number and normally in the range of 0.05 to 0.2. A passive decap, as shown in Fig. 1(a), provides a charge of $kC_{decap}V_{DD}$ to the supply. In a CBD, as shown in Fig. 1(b), however, the charge provided by the CBD circuit in one clock cycle can ideally be up to $C_{decap}\Delta V_{clk} = C_{decap}V_{DD}$, where ΔV_{clk} is the clock swing. Clearly, over one clock cycle, the CBD provides 5X-20X more charge than a same-area passive decap, depending on the actual noise level. From another perspective, the CBD circuit can boost the local supply voltage to $2V_{DD}$ ideally, but passive decaps cannot.

The circuit in Fig. 1(b) suffers from clock feedthrough problems on the falling edge of the clock. When the Clk signal rises from 0 to V_{DD} , the supply is boosted to $2V_{DD}$ ideally due to capacitance feedthrough. Then, nearby user logic circuits switch, resulting in certain amount of charge to withdraw from the supply, reducing the supply voltage by ΔV . When the Clk signal falls from V_{DD} back to 0, the supply voltage drops from $2V_{DD}-\Delta V$ to $V_{DD}-\Delta V$, which may not be acceptable if ΔV is large. This problem can be solved by adding additional circuitry as shown in Fig. 2(a). Two diodes are inserted at node B1, one connected to the clean supply and the other to the noisy supply. Without the connection to the clean V_{DD} , when the clock is low, B1 stays at roughly V_{SS} since the current flow from V_{DD} to B1 is prevented by the diode, D2. When the clock goes high, B1 rises to V_{DD} . This boost in voltage will not trigger current flow from B1 to the supply because both B1 and the supply are at the same level ($\sim V_{DD}$). Thus, the voltage at B1 should be around V_{DD} when the clock is low. This ensures that the voltage at B1 can reach about $2V_{DD}$ when the clock goes high and the noisy supply can be charged. To achieve that, access to a clean supply of V_{DD} is needed through D1.

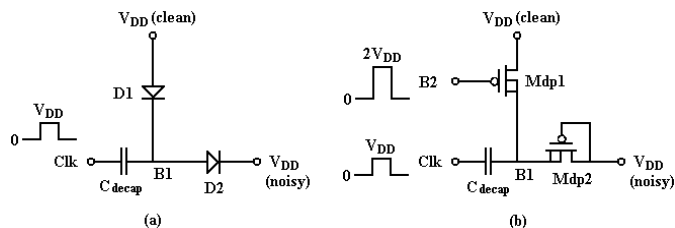


Fig. 2. (a) Diode inserted CBD and (b) one possible MOS implementation.

Assuming there is one threshold voltage V_T drop across each diode, the operation of the CBD circuit, as illustrated in Fig. 2(a), is follows. When Clk is at 0, the noisy supply node is assumed to be at V_{DD} , while B1 is charged at $V_{DD}-V_T$ from the clean supply. When Clk rises to V_{DD} , B1 rises to $2V_{DD}-V_T$ at the same time. As a result, the noisy supply node is

3.8mW. Note that this dynamic power is not wasted, but rather transferred between the supply nodes. Only the power consumption of $65\mu\text{W}$ from the ring oscillator can be considered as power overhead, which is merely 0.2%.

When determining the size of the buffer chain, C_{decap} was chosen to be 700pF. Assuming a fixed edge delay, the size of buffer required is proportional to the decap value. If a smaller decap is used, the buffer size can be made smaller to dissipate less power. This power drawn from the clean supply node is critical so that the supply noise caused by the ring oscillator and the buffer chain should not rise beyond the noise budget in its localized region. That is, the goal of generating the “Clk” signal from a clean V_{DD} is to provide charge from the clean supply that is not connected to the main system clock or any important circuitry. The designer must ensure that the clean supply itself does not become excessively noisy so that the local supply integrity is compromised.

C. Overall CBD Design

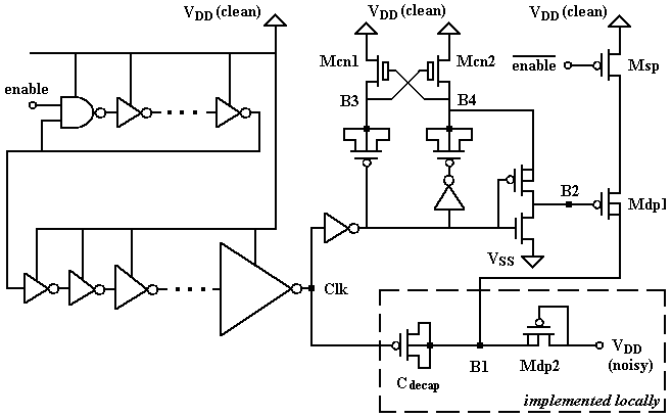


Fig. 6. Complete circuit diagram of charge-borrowing decap.

The complete charge-borrowing decap circuit is shown in Fig 6. An *enable* signal is provided to turn off the CBD for test purposes. When the enable signal is low, the transistor M_{sp} is off, preventing current flow from the clean supply. The decap is implemented using PMOS transistors. When enabled, the voltage at B2 varies from 0 to $2V_{\text{DD}}$. The gate-source capacitance of M_{dp1} creates additional noise on the clean supply node due to clock feedthrough. The existence of M_{sp} provides shielding to the clock feedthrough to reduce this noise. The practical boosted voltage is $2V_{\text{DD}} - |V_{\text{thp2}}|$, while the charge provided per cycle is $C_{\text{decap}}V_{\text{DD}}$. Note that the ESD concerns on the thin-oxide decap should be addressed by proper sizing of the two transistors, M_{dp1} and M_{dp2} .

As described earlier, after a local hot spot is identified, the nearby passive decaps can be replaced by a CBD. Only the transistor M_{dp2} needs to be implemented locally. Other circuits showing in Fig. 6 can be located away from the hot spot but near a clean supply node. The actual placement of the ring oscillator and the buffer chain will depend on the floorplan and location of power pins of the chip itself. Two global interconnects may be required to connect the two parts of circuits at node Clk and B1. Compared to the size of the passive decap, the size of M_{dp2} is negligible, resulting in a very small area overhead in the local area.

III. CHIP DESIGN AND EXPERIMENTAL RESULTS

To validate our design, a test chip was fabricated in a 1V-core STM 90nm process. The test chip setup and microphotograph are shown in Fig. 7 and 8, respectively. An active decap [4] of the same size was also implemented for comparison. For test purposes, the Clk signal was not generated from the ring oscillator, but from an external clock that was synchronized with the user logic clock.

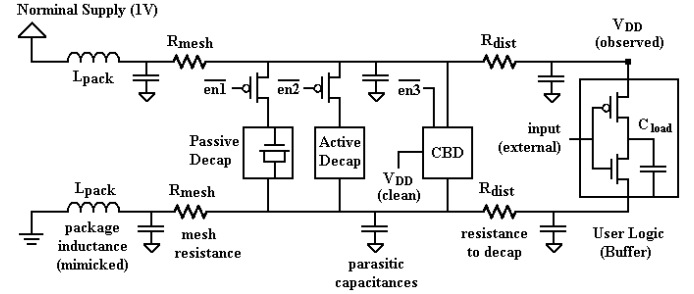


Fig. 7. Test chip setup in a 90nm STM process.

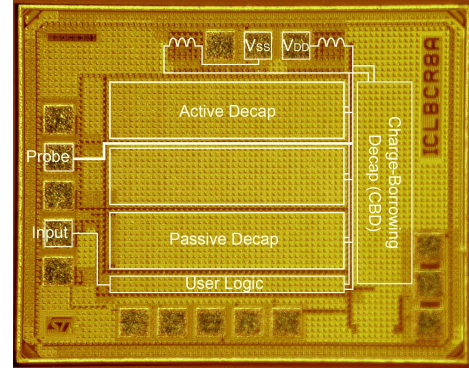


Fig. 8. Annotated microphotograph of the test chip.

In order to observe signals near the logic block, the supply variations were measured directly with probes. It is understood that the package inductance is an important source of power supply noise [8]. Since we did not use a packaged chip, two on-chip spiral inductors were implemented to mimic the package inductances, one on the supply path and the other on the return path. The value of the spiral inductors is close to a typical wire-bond package inductance.

The layout area for the passive decap, active decap, and CBD is about $0.6 \times 0.15 = 0.09\text{mm}^2$ each. The total chip area is $1.1 \times 0.86 = 0.95\text{mm}^2$. The decap circuits are placed about 0.6mm away from the user logic, in which a large buffer with a large capacitive load was used to create supply noise, with the input controlled by an external clock signal. The size of the passive decap was chosen to be only a few times larger than the capacitive load to create a $\sim 100\text{mV}$ voltage drop for the experiments. The clock frequency was controlled externally using an Agilent 86130A analyzer. The probed pad of the supply node was connected to an Agilent DSO81304A oscilloscope to measure the voltage waveforms.

The average V_{DD} voltage per clock cycle is measured and compared since it is known to strongly influence the critical path delay of logical circuits [9][10]. A collection of 9 sample chips were tested. The improvement across the sample space is shown in Fig. 9, where the clock frequency was fixed at

1GHz for this test. The two sample chips that are in the fast process corner can be identified by correlating with simulation. In Fig. 9, the average supply voltage varies significantly mainly due to the random process variation on R_{mesh} and L_{pack} , which determines the IR drop on the supply rails. Note that the supply noise reduction improvement by using the CBD is rather consistent under process variations across dies, which indicates the robustness of the design. The sample chip that provides the best improvement was used for further analysis.

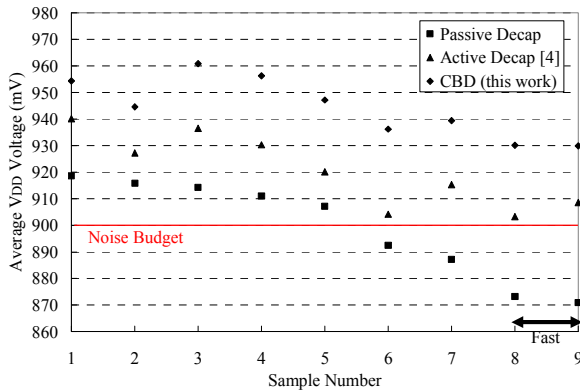


Fig. 9. Scatter plot comparing average V_{DD} for the tested sample chips.



Fig. 10. Superimposed waveforms of a test chip on a 1GHz clock.

The waveforms of this test chip with a 1GHz clock are depicted in Fig. 10. The dark gray (blue in color) curve is when the CBD is on, and the light gray (red in color) curve is when the passive decap is on. The two curves are superimposed. Clearly, the supply voltage returns to high when extra charge is fed through from the clean supply on the rising edge of the clock, improving the average V_{DD} level.

Fig. 11 shows the impact of changing the external input frequency from 100MHz to 1.5GHz. Two solid trend lines are provided corresponding to the CBD and the passive decap. The gap between the two trend lines widens indicating that the benefit of using the CBD increases as frequency increases. At 1.5GHz, the gap does not diminish, showing that the CBD is suitable for today’s high-speed ASICs and medium-speed custom designs. The test chip validated that the CBD has a maximum improvement of 93mV (or about 53% less noise) at 1.5GHz. Across the frequency range from 100MHz to 1.5GHz, using the CBD reduces the supply noise from 42% to 55%,

hence resolves the issue on local hot-spot violations. Note that the CBD outperforms a recently published work [4] by roughly 20% in terms of reducing supply noise.

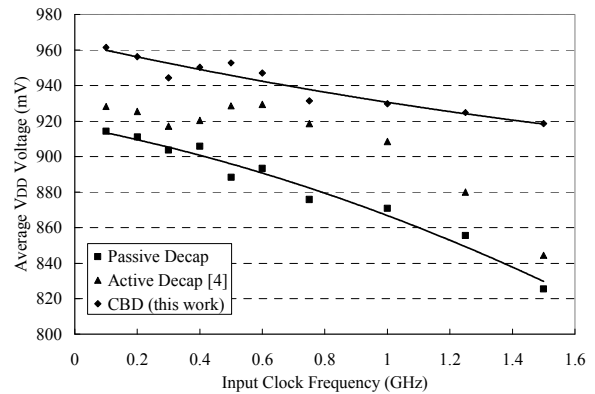


Fig. 11. Measured average V_{DD} voltages at different clock frequencies.

IV. CONCLUSION

This paper proposed a novel charge-borrowing decap (CBD) circuit that provides significantly better supply noise reduction than passive decaps. It can be used to remove local IR -drop violations as a drop-in replacement to passive decaps. The CBD delivers more charge and an increased supply boost for a wide range of clock frequencies. Measurement results from a 90nm test chip show a noise reduction improvement of 42%-55% over passive decaps, operating from 100MHz to 1.5GHz.

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