SOHAIB MAJZOUB

sohaib.majzoub@ieee.org
System-On-Chip Research Group
2356 Main Mall - Room #332
The University of British Columbia
Vancouver, BC V6T 1Z4
Phone: 604-822-6848

4038 W. 32nd Avenue
Vancouver, BC V6S 1Z6
Canada
Cell: 778-689-6459

EDUCATION

The University of British Columbia (UBC), Vancouver, Canada 2005-2010
Ph.D. in Electrical & Computer Engineering, (PhD Tuition Fee Award)

- Area of Specialization: System-Level Power Optimization & Modeling under Process, Voltage and Temperature Variations for Multi-Processor System-on-Chip (MPSoC).

Swiss Federal Institute of Technology (EPF),) Lausanne, Switzerland 2003-2004
Pre-Doctoral Degree in Computer, Communications & Information Sciences,
(Doctoral School Fellowship).

- Area of Specialization: Reconfigurable Processor Design, soft Datapath for ARM Instruction Based Processor

The American University of Beirut (AUB), *Beirut, Lebanon* 2001-2003
Masters in Computer & Communication Engineering, (Graduate Assistantship)

- Area of Specialization: Performance Analysis of Multimedia Applications on Reconfigurable Hardware, MorphoSys.

Beirut Arab University (BAU), *Beirut, Lebanon* 1995-2000
Bachelor in Electrical Engineering, Computer Section

RESEARCH AND TECHNICAL EXPERIENCE

PhD Research and Technical Projects 2008 - Present
University of British Columbia, Vancouver, BC

Project: Low Power Design of Multi-processor System-on-Chip (MPSoC) with Thousands of Cores under Process, Voltage, and Temperature (PVT) Variations.
Energy optimization techniques at the system level, namely Voltage and Frequency Scaling (VFS), threshold Voltage Body Biasing (VBB), and power gating techniques were utilized to save on dynamic as well as static power in Many-Core architectures with massive number of cores. The evaluation platform was considered under the influence of Process, Voltage and Temperature (PVT) variations, which are common in small-featured technologies, 45nm and beyond.

- Power saving techniques were applied including Voltage and Frequency Scaling (VFS), and Voltage Island formation to save on dynamic power, and body biasing to save on static power.
- Process, voltage and temperature variations were considered during optimization. Within die systematic as well as random variation were modeled using multivariate normal distributions with spherical correlation structure. HotSpot© was used to evaluate the core temperature variations. A resistive power grid network was modeled to capture core voltage variations
- Proposed a structural advantage in forming voltage islands in massive multi-core designs. The proposed technique reduces frequency discrepancy among cores due to PVT.
- Proposed a very fast voltage selection technique, Removal Cost Method (RCM), that provides near optimal results.
- The optimization platform was built using MATLAB. The variables in the delay/power models were extracted from 45nm.
- More than 35% power savings were achieved by using the new proposed techniques.
- On-going work includes exploring and investigating multi threshold voltage in improving the static power savings. More examination of the voltage island shapes and/or constrains and their impact on power grid design.
- Future work will include moving towards more aggressive technologies, i.e. 22nm and beyond.

Research Assistant – System-on-Chip Research Lab 2007 - 2008

Project: RTL Delay Macro-Modeling with Vt and Vdd scaling under Process, Voltage, and Temperature Variations. (in collaboration with the VLSI System Design group, Ritsumeikan University, Japan.)
Critical path delay estimation model under PVT was built by using the alfa and mobility constants in the Alfa-Delay model as fitting parameters. The model parameters are first extracted from NAND, NOR, and INV chains simulated in HSPICE© using different TSMC PVT variations libraries. The model was then validated on real circuits, ITC'99 benchmarks. The benchmarks are synthesized from RTL to gate-level using dc_shell and then simulated to determine the critical path delay with different TSMC process libraries using pt_shell, PrimeTime©. The model was able to match PrimeTime© results with error margin 6.77%.

Project: Instruction-Based Voltage Island Formation in SIMD MPSoCs. 2006 - 2007
Power management technique based on instruction Power/Delay profiling in a SIMD type MPSoC architectures. In a multi-core SIMD platform, fast instructions are routed to cores with low supply voltage and slow instructions are routed to cores with high supply voltage.

- A simple ALU with logic, arithmetic, and multiply and accumulate instructions was designed and realized at the RTL level. The ALU design was written in VHDL.
- PrimeTime© from Synopsys© is used to major the timing characteristics of each instruction. Specifically, the command SET_CASE_ANALYSIS is used to measure the path delay.
- Encounter© from Cadence© is used to back-annotate the parasitic capacitances to the design to have accurate delay measurements.

- PrimeTime PX© is used to measure the power consumed during the execution of each instruction. To generate the signal activity, NCSIM© from Cadence© is used to generate the VCD files used later with UPDATE_POWER command, PrimeTime©.

Tools Utilized:

Digital Design Flow (0.18µm, 90nm, 65nm and 45nm technologies):

- Design, with VHDL, of Arithmetic Logic Unit (ALU) that includes arithmetic and logic operations, carry-save multiplier and a divider.
- Synthesizing the RTL netlist into Gate-level netlist using dc_shell (Synopsys©)
- Timing Analysis using pt_shell (PrimeTime© SI, Synopsys©)
- Power Analysis using pt_shell (PrimeTime© PX, Synopsys©)
- Layout and back-annotation of parasitic capacitances using Encounter© (Cadence©)

Masters' Projects:

- In EPFL, I worked in the processor architecture lab (LAP) in implementing a soft datapath for ultra low power, ARM-Instruction-based, processor called URLAP. The datapath can be dynamically reconfigured and customized to improve the application performance. The project was part of the MegaWatch project. A small watch developed for sport and medical applications.
- In AUB, I worked in performance analysis of application mapping in areas of digital signal processing (FFT, 2D convolution, etc), digital image processing (lossless image compression, computer graphics algorithms), and cryptographic applications (TWOFISH, RIJNDAEL, MD5) on dynamical reconfigurable architecture, MorphoSys. The work was a joint project with University of California at Irvine and Morpho Technologies Inc. Irvine. Exhaustive analysis and recommendations about hardware improvements were provided to improve the system.

PUBLICATIONS

Refereed Journal Publications:

S. Majzoub, R. Saleh, S. J.E. Wilton and R. Ward "Energy Optimization for Many-Core Platforms: Communication and PVT Aware Voltage-Island Formation and Voltage Selection Algorithm," to appear in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE-TCAD), 2010*.

S. Majzoub, H. Diab "MorphoSys Reconfigurable Hardware for Cryptography: The Twofish Case," to appear in *Journal of Supercomputing (JSC), 2010*.

S. Majzoub, and H. Diab, "Instruction-Set Extension For Cryptographic Applications On Reconfigurable Platform" Special Issue on Advances in Circuits and Systems for Large Scale Integration, in *The Journal of Circuits, Systems, and Computers*, (JCSC) Vol. 16, No. 6, 2008.

Refereed Conference Publications:

S. Majzoub, R. Saleh, S. J.E. Wilton, and R. Ward "Simultaneous PVT-Tolerant Voltage-Island Formation and Core Placement for Thousand-Core Platforms," *International Symposium on System-on-Chip (SoC'09),* October 5-7 2009, Tampere, Finland.

S. Majzoub, R. Saleh, S. J.E. Wilton, and R. Ward "Removal-Cost Method: An Efficient Voltage Selection Algorithm for Multi-Core Platforms under PVT," *22nd IEEE International System-on-Chip Conference (SoCC'09),* September 9-11 2009, Belfast, UK.

S. Majzoub, R. Saleh, and R. Ward, "PVT Variation Impact on Voltage Island Formation in MPSoC Design" *The 2009 International Symposium on Quality Electronic Design (ISQED'09)*, March 16-18, 2009, San Jose, CA, USA.

S. Majzoub, H. Diab, "Mapping and Performance Analysis of Lookup Table Implementations on Reconfigurable Platform," *IEEE/ACS International Conference on Computer Systems and Applications (AICCSA'07)*, Le Méridien Amman Hotel, Amman, Jordan, May 13-16, 2007 pp.513-520.

S. Majzoub, H. Diab, "Instruction-Set Extension for Cryptographic Applications on Reconfigurable Platform" *The 6th International Workshop on System-on-Chip for Real-Time Applications, (IWSoC'06)*, Cairo, Egypt, December 27-29, 2006.

S. Majzoub, R. Saleh, and H. Diab, "Reconfigurable Platform Evaluation Through Application Mapping And Performance Analysis," *The 6th IEEE International Symposium on Signal Processing and Information Technology (ISSPIT'06),* August 27-30, 2006, Vancouver, Canada.

M. Al-Khalidy, H. Diab, and **S. Majzoub**, "MorphoSys implementation of MD5 hash algorithm," *International Conference on Current Issues in Business and Information Technology*, Beirut, Lebanon, May 21-22, 2004.

H. Diab, and **S. Majzoub**. "Linear Filtering Algorithm Using Reconfigurable Computing." *The ACS/IEEE International Conference on Computer Systems and Applications (AICCSA'03)*, Tunisia, July 14-18, 2003.

S. Majzoub, and H. Diab. "Mapping and Performance Analysis Of The Twofish Algorithm On MorphoSys." *The ACS/IEEE International Conference on Computer Systems and Applications (AICCSA'03)*, Tunisia, July 14-18, 2003.

I. Damaj, **S. Majzoub** and H. Diab. 2D and 3D Computer Graphics Algorithms under MorphoSys. *The 12th International Conference on Field Programmable Logic and Applications (FPL'02)*, Montpellier, France 2002, Springer-Verlag, 1076-1079.

Theses:

S. Majzoub, "Power Optimization for Many-Core Platforms under PVT," Ph.D. Thesis (to be completed by early 2010).

S. Majzoub, "Reconfigurable Datapath for Ultra Low Power URLAP Processor on Virtex-II FPGA Platform." Masters, Thesis (EPFL).

S. Majzoub, "Performance Analysis of Parallel Computing Algorithms Using Reconfigurable Computing." Masters. Thesis (AUB).

TEACHING EXPERIENCE:

University of British Columbia:

EECE 496: Engineering Project 2005, 2008
- *Assisted a project to build an emulator for MorphoSys (2005)*
- *Assisted a project to do application analysis of StepNP (system level simulator) (2008)*

EECE 356: Electronic Circuits II, 2007, 2008 and 2009
- *Teaching Assistant & Lab Instructor*

EECE 259: Introduction to Microcomputers 2008
- *Teaching Assistant*

American University of Beirut:
Introduction and assistance for Master degree Theses and Final year projects for both the Graduate and Undergraduate Levels for CCE and EE students:
- Undergraduate Final Year Project: "Enhancing the Performance of Modular Dynamics Simulation on MorphoSys M1."
- Master Degree Thesis: "Routing and Security Algorithms on MorphoSys."
- Undergraduate Final Year Project: "Performance Evaluation of Parallel Algorithms on MorphoSys Reconfigurable System for IPv6 and Digital Signal Processing Algorithms"

COMPUTER SKILLS

- Hardware tools (Cadence©: Analog Artist©, Encounter©; Synopsys: dc_shell, pt_shell, SPICE©)
- Hardware programming languages (Verilog, VHDL)
- Technical programming languages (MATLAB©)
- Programming languages (C/C++, HTML, PASCAL, BASIC)
- Operating systems (Unix (Solaris), Linux (Debian), Mac OS, MS Windows)

AFFILIATIONS

Student Member of IEEE	1998 - Present
Student Member of IEEE Computer Society	1998 - Present
Student Member of ACM	2004 - Present
Member of the UBC System-on-Chip Research Group	2005 - Present
Volunteer Reviewer for DAC	2008, 2009, and 2010