Effect of Traffic Localization on Energy Dissipation in NoC-based Interconnect

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Abstract

Multiprocessor system-on-chip (MP-SoC) platforms are emerging as an important trend of SoC design. Scaleable communication-centric interconnect fabrics such as networks-on-chip (NoCs) possess many features that render them particularly attractive for enabling such platforms. In particular, due to their modular structure, NoCs can exploit locality in communication and reduce the need for long global wires, thereby significantly lowering the energy dissipation without compromising system throughput. In this paper, we study the effect of traffic localization on the energy dissipation of different NoC interconnect architectures. To quantify the degree of energy savings, we introduce the energy dissipation versus throughput as a useful metric. Through system level simulation, we show that energy reductions of up to 50% can be achieved by exploiting locality in communication.

Keywords: NoC, Traffic Localization, Throughput, Energy, Modularity, Interconnect Infrastructure.

1. INTRODUCTION

Recent publications [1] [2] claim that the emergence of system-on-chip (SoC) platforms consisting of a large number of embedded processors is imminent. The design of these platforms will be governed by wiring considerations and power constraints [3]. In view of achieving lower energy dissipation, they should exhibit explicit parallelism, significant pipelining, and a relatively high degree of modularity. These design characteristics will generally reduce the requirement for long global wires, which tend to be a dominant factor for energy dissipation in such large systems [2]. According to ITRS (2003) [3], such system designs should also adhere to networking and distributed computation paradigms. A key element of such multiprocessor SoC (MP-SoC) platforms [1] is the interconnect topology. To date, the most frequently used on-chip interconnect architecture is the shared-medium arbitrated bus. The network-on-chip (NoC) paradigm, e.g., [4] [5] [6] is emerging as a viable and attractive alternative to this classical model for many reasons.

Generally, a NoC interconnect topology resembles the interconnect architecture of high-performance parallel computing systems [2]. The common characteristic of such architectures relative to MP-SoC is that the functional IP blocks communicate with one another via intelligent switches. The switch-based architectures offer the advantage that the switches, along with the inter-switch wire segments, lead to a highly-modular and structured interconnect infrastructure which, in turn, allows a higher degree of spatial locality with regard to the inter-block communications. Consequently the functional mapping should be performed so as to exploit the advantages of spatial locality, i.e., the blocks that communicate more frequently should be placed closer to each other. This will reduce the use of long global paths and the energy dissipation. Here, through modeling and simulation we seek to quantify the amount of potential energy savings by studying the effects of different factors of traffic localization on NoC architectures.

1.1 Related work

A few on-chip micro network proposals for SoC integration can be found in the literature. The authors of [5] and [8] proposed mesh-based interconnect architectures. These architectures consist of an \( m \times n \) mesh of switches interconnecting computational resources (IPs) placed along with the switches. In [5], Dally et al. proposed the use of a torus interconnect architecture. A variation of the torus architecture, which eliminates the use of long wraparound wires, called a folded torus, is described in [9]. Guerrier and Greiner [6] proposed the use of a fat tree-based interconnect (SPIN) and system level design issues. In [10], the authors described an interconnect architecture based on a butterfly fat tree (BFT) for a networked SoC, as well as the design of required switches and addressing mechanisms. In [11], the power consumption of switch fabrics for network routers has been discussed and the concept of bit-energy as a measure of power efficiency was introduced.

2. MP-SoC INTERCONNECT ARCHITECTURES

Instead of building a multiprocessor (MP) SoC around an ad-hoc interconnection of multiple buses, different parallel computing architectures can be adopted in the SoC domain. Most of the NoC architectures proposed to date evolved from earlier parallel processing structures, e.g., [4] [5] [6] [8] [10]. Fig. 1 summarizes some of the proposed NoC architectures that are evaluated in this paper. For uniformity, the wormhole routing technique [14], where data packets are divided into fixed length flow control units (flits), is adopted. A packet is divided into a header flit containing routing and flow control information, one or more data flits, and a tail flit indicating the end of packet.

In multiprocessor platforms throughput is one of the key parameters that governs the computational performance of the system. In addition, in the SoC domain, the issue of energy dissipation of the interconnect architectures is of prime importance. We use throughput and energy dissipation as a basis for comparison of the different NoC architectures, as described below.

2.1 Message Throughput

Typically, the performance of a digital communication network is characterized by its bandwidth in bits/sec. However, we are more concerned here with the rate that message traffic can be sent across the network and so throughput is a more appropriate metric. Throughput can be defined in a variety of different ways depending on the specifics of the implementation. For message passing systems, we can define message throughput, \( TP \), in units of flits per cycle per IP as follows:
where Total messages completed refers to the number of whole messages that successfully arrive at their destination IPs, Message length is measured in flits, Number of IP blocks is the total number of IP blocks present in the system, and Total time is the time (in clock cycles) that elapses between the occurrence of the first message generation and the last message reception.

2.2. Energy dissipation in a NoC-based SoC

When flits travel through the interconnection network, both the inter-switch wires and the logic gates in the switches toggle, resulting in energy dissipation. The flits from the source nodes need to travel over multiple hops, with each hop consisting of a switch and wire segments between switches, to reach their respective destinations. The energy per flit per hop is given by

\[ E_{\text{hop}} = E_{\text{switch}} + E_{\text{interconnect}} \]  

(2.1)

The energy dissipated in transporting a flit through \( h \) hops from source to destination can be calculated as

\[ E_{\text{flit}} = \sum_{j=1}^{h} E_{\text{hop},j} \]  

(2.2)

Let \( P \) be the total number of flits transported, \( n \) be the number of bits in a flit and let \( E_{\text{bit}} \), be the energy dissipated by the \( i^{th} \) flit, where \( i \) ranges from 1 to \( P \). The average energy per bit, \( E_{\text{bit}} \), can then be calculated according to the following equation:

\[ E_{\text{bit}} = \frac{1}{P \cdot n} \sum_{i=1}^{P} E_{\text{bit},i} \]  

(2.3)

To compute the term \( E_{\text{hop},j} \) using Eqn. (2.1), we determined the energy dissipated in each switch, i.e., \( E_{\text{switch}} \), by running Synopsys\textsuperscript{TM} Prime Power on the gate-level netlist of the switch blocks. To determine the interconnect energy, we used \( E_{\text{interconnect}} = \alpha C_{\text{interconnect}} V_{DD}^2 \), where \( \alpha \) is the signal activity factor, determined from Prime Power. The capacitance of each inter-switch stage, \( C_{\text{interconnect}} \), is calculated taking into account the specific layouts required to support each of the different topologies; that is, \( C_{\text{interconnect}} \) can be estimated according to the following expression

\[ C_{\text{interconnect}} = C_{\text{wire}} \cdot w_{a+1,a} + N \cdot (mC_G + mC_J) \]  

(2.4)

where \( C_{\text{wire}} \) is the wire capacitance per unit length, and \( w_{a+1,a} \) is the wire length between two consecutive switches; \( C_G \) and \( C_J \) are the gate and junction capacitance of a minimum size inverter, respectively, \( N \) denotes the number of inverters (when buffer insertion is needed) in a particular inter-switch wire segment and \( m \) is their corresponding size with respect to a minimum size inverter. When calculating \( C_{\text{wire}} \) we considered the worst-case switching scenario, i.e., the case where the two adjacent wires switch in the opposite direction of the signal line simultaneously [12].

3. SIMULATION ENVIRONMENT

We developed a flit-level, event-driven, wormhole routing simulator to study the energy dissipation characteristics of the NoC architectures. In our experiments, the traffic injected by the functional IP blocks followed self-similar distributions [13]. The injection load measured in flits/cycle/IP characterizes the traffic injection process. The self-similar distribution was found to be a realistic approximation to real-world SoC scenarios [13]. For example, self-similar traffic has been observed in the bursty traffic between on-chip modules in typical MPEG-2 video applications [13]. Each simulation was initially run for 1000 cycles to allow transient effects to stabilize and subsequently executed for another 20,000 cycles. To calculate average energy, we associated an energy value \( E_{\text{switch}} \) and \( E_{\text{interconnect}} \) with each switch and interconnect segment, respectively. The average energy dissipation in transmitting a bit through the NoC was calculated according to equation (2.3).

High message throughput is one of the most desirable characteristics of an interconnect infrastructure. However, the highest performing architectures may exhibit unacceptably high energy dissipation profiles. In this paper, we are advocating the use of the energy versus throughput as a meaningful measure of efficiency of various NoC architectures.

4. EXPERIMENTAL RESULTS AND ANALYSIS

To evaluate and compare the energy dissipation characteristics of different NoC-based architectures of Fig. 1, we considered systems consisting of different numbers of IP blocks.
and mapped them to the interconnect architectures under consideration. We studied the effect of two cases of spatial distribution of traffic. In the first case, the traffic was uniformly distributed among all the destinations, while in the second case, the traffic was localized to different degrees of localization. In all our experiments, we assumed a self-similar injection process. To specifically study the effect of system size on the energy dissipation under varied traffic localization, we considered three different system sizes, i.e., 16, 64, and 256 IP blocks, numbers believed to be illustrative of what could be considered as small-, medium-, and large-scale MP-SoC platforms. In our routing schemes we use distributed source routing; i.e., the source node determines only its neighboring nodes that are involved in message delivery. For the tree-based architectures, the routing algorithm applied is the least common ancestor (LCA) and, for Mesh and Folded Torus, we apply the e-Cube (dimensional) routing [14]. In all the architectures the switches have four virtual channels per physical link; we developed their VHDL models and synthesized them using a fully static, standard cell-based approach for a 0.13 μm CMOS technology library.

We considered a system with 64 IP blocks as a representative case for illustrating the nature of throughput and energy dissipation as a function of injection load. Throughput is the maximum traffic accepted by the network and it relates to the peak data rate sustainable by the system. Ideally, accepted traffic should increase linearly with injection load. However, due to the limitation of routing resources (switches and interconnect wires) accepted traffic will saturate at a certain level of injection load. The throughput characteristics of each NoC architecture under consideration are shown in Fig. 2. These are reported as a function of injection load for random traffic uniformly distributed among all the destinations, for a system size of 64 IP blocks.

The average bit energy dissipation $E_{bit}$ when data is transmitted between a pair of source and destination IP blocks for the same 64 IP system size and the same traffic scenario as above is shown in Fig. 3. The bit energy dissipation follows the same saturating trend as does the throughput. The Torus and Folded Torus have very similar throughput characteristics, but the energy dissipation in the Folded Torus is less, mainly due to the absence of long wraparound wires. From Fig. 3 we can infer that the architecture with higher degree of connectivity like Fat Tree has greater average energy dissipation at saturation than the others though it provides higher throughput.

The assumption of uniformly distributed traffic is obviously not a very realistic one. In a true MP-SoC environment, different functions would map to different parts of the SoC and the traffic patterns would be expected to be localized to different degrees.

**Figure 2: Throughput characteristics**

The relative amount of energy savings for different localization factors is shown in Fig. 6. To have a consistent comparison, we kept the system throughput at the same level for all the architectures, while varying the amount of localized traffic. The relative amount of energy savings is not significantly affected by system size. When the factor of localization is varied from 0.3 to 0.8, the bit energy savings relative to the uniformly distributed traffic scenario vary from 20% to 50%, independently from the system size in terms of number of IPs. This trend is observed for all the NoC topologies under consideration. This brings out one of the major advantages of these modular NoC architectures, that is, reducing the degree of global communication improves the energy efficiency of the systems without compromising system throughput.

**Figure 3: Average Bit Energy dissipation $E_{bit}$ as a function of the injection load (uniform traffic)**

We therefore studied the effect of traffic localization on energy dissipation and considered the illustrative case of spatial localization where local messages travel from a source to the set of the nearest destinations. In the case of BFT and Fat Tree, localized traffic is constrained to within a cluster consisting of a single sub-tree while, in the case of Mesh, Torus and Folded Torus, it is constrained to within the four destinations placed at the shortest Manhattan distance [14]. We define the localization factor as the ratio of local traffic to total traffic. For example, if the localization factor is 0.3, then 30% of the traffic generated by an IP occurs within its cluster while the rest of the traffic is uniformly distributed in the remainder of the entire SoC.

The variation of bit energy dissipation with injection load alone is not an indicative measure of energy efficiency of any given NoC architecture. The bit energy dissipation versus throughput is a better indicator that enables a more significant comparison as it effectively expresses the dissipation with respect to data processing capability.

Fig. 4 shows the variation of bit energy as a function of system throughput for three different system sizes, under uniformly distributed traffic scenarios. It can be inferred from Fig. 4 that the nature of bit energy variation with throughput remains approximately the same with various system sizes, only the absolute value differs.

To evaluate the advantage of traffic localization on energy dissipation, we studied the bit energy vs. throughput characteristics for different degrees of localizations. Fig. 5 shows the variation of bit energy with throughput for a localization factor of 0.5 for three different system sizes. From Fig. 5, as a result of traffic localization, system throughput increases while the bit energy dissipation decreases compared to the case of uniformly distributed traffic. From Figs. 4 and 5, we can infer that for a given throughput, an increased degree of localization results in a reduced bit energy dissipation, as one would expect.

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5. CONCLUSIONS

NoCs are emerging as the suitable interconnect architectures for MP-SoC platforms. Their energy dissipation is a characteristic of critical importance. We showed that it is strongly correlated to the system throughput and spatial distribution of traffic. The modularity of these NoC architectures can be exploited to reduce the amount of global communication. The locality in communication enhances the system throughput and as well reduces the average energy dissipation. System size does not have significant impact on the reduction of energy dissipation due to traffic localization. Here, we have quantified these features for various NoC contenders. For this evaluation, we introduced energy vs. throughput as a relevant metric. We showed that the spatial localization of traffic can significantly decrease the energy dissipated by the NoC interconnect fabrics, by up to 50% from our set of experiments.

6. REFERENCES