International Journal of High Speed Electronics and Systems
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FULL-CHIP POWER-SUPPLY NOISE: THE EFFECT OF ON-CHIP POWER-RAIL INDUCTANCE

C.W. FOK
Department of Physics and Astronomy, University of British Columbia
Vancouver, BC V6T1Z4, Canada

and

D.L. PULFREY
Department of Electrical and Computer Engineering, University of British Columbia
Vancouver, BC V6T1Z4, Canada

Received (received date)
Revised (revised date, if applicable)
Accepted (accepted date, if applicable)

The importance of on-chip power-rail inductance in generating delta-I power-supply noise is examined in this paper using systematic circuit simulation of the complete integrated-circuit power net. This source of noise is compared to the resistive IR drop in the net, and to the delta-I noise due to both high-inductance- and low-inductance-bonding packages. Results are presented for a typical on-chip power net in 0.18 μm CMOS technology, and it is demonstrated that the inductance of this on-chip power net is the dominant contributor to the full-chip power-supply noise. The simultaneous switching events which produce the triggering current transients for the delta-I noise are taken to arise from core-logic switching; the mitigating, de-coupling role of the capacitance of non-switching gates within the core-logic block is considered.

1. Introduction

As silicon integrated-circuit sizes increase, the long, on-chip power lines become important sources of resistance and self- and mutual-inductance. Also, as silicon MOSFET sizes decrease, the circuit density increases, with the result that larger currents are demanded and larger current transients appear. These two size-related phenomena, coupled with the trend of decreasing power-supply voltage, lead to the possibility of significant power-supply noise due to both resistive voltage drops and inductive voltage changes. In this paper, the full-chip power-supply noise is considered, and particular attention is paid to determining the importance of the contribution to this noise of the inductance of the on-chip power net. The intention is to resolve the issue of whether the on-chip inductance is really important, in view of the presence of significant inductance in the bonding package: there is presently some difference of opinion on this [1,2,3].

Our approach is to perform systematic circuit simulations of a full chip comprising a representative, 0.18 μm CMOS power system, with either wire-bond- or flip-chip-

packaging. The impedance of the full-chip power network is simulated in its entirety, and also by considering each of the impedance components separately, namely: package inductance, on-chip resistance, and on-chip inductance. This approach reveals that it is necessary to consider the inductance of the on-chip power net if the power-supply noise (PSN) is not to be seriously underestimated.

The ΔI component of PSN originates in the massive, simultaneous switching of many on-chip devices. Here, we consider this switching to take place in core-logic blocks, and we use a Monte-Carlo approach to generate a switching pattern that gives rise to off-chip, power-supply currents that are typical of modern processors. Within the logic blocks considered in this work, only 20% of the gates switch in a given cycle. Consideration is given to the de-coupling role that the capacitance of the non-switching gates within the block might play in providing some of the current demanded by the switching gates, thereby reducing the current that needs to be delivered via the inductive power-supply net.

2. Methodology

Figure 1 illustrates the system considered: it comprises an off-chip power supply, bonding-package inductances, an inductively coupled on-chip power net, and blocks of logic gates. The capacitance of the power net is also considered, but it has been found to have negligible effect on the simulated power-supply noise.

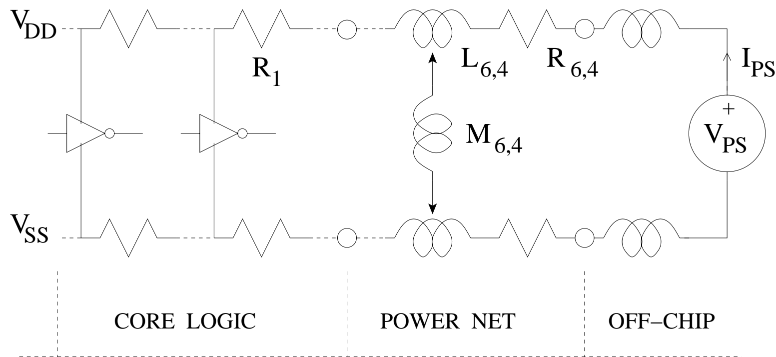

Fig. 1. Full-chip schematic. $R_{6,4}$ and $L_{6,4}$ refer, respectively, to the resistance and self-inductance of power lines in Metals 6 and 4. $M_{6,4}$ is the mutual inductance of the network of Metal 6 and Metal 4 lines. R_1 is the resistance of the Metal 1 lines.

In this work, the network size is large enough to ensure a statistically meaningful result, but it is also small enough to allow the simulation of PSN to be accomplished in a reasonable time (several hours on a SUN Ultra 10 workstation). Specifically, wire- and flip-chip-bonding schemes are applied to 15 pairs of V_{DD}/V_{SS} lines arranged in a parallel fashion in Metal 6. These lines are connected at the appropriate crossover points to 15 pairs of orthogonal lines in Metal 4 which, in turn, are connected to 40 pairs of orthogonal, resistive power lines in Metal 1. This

is a typical power net arrangement [4], and, with the wire specifications listed in Table 1, leads to a chip area of 36.9 mm^2.

Table 1. Metal layer specifications.

Metal	Resistivity (Ω/sq.)	Width (μm)	Height (μm)	Spacing (μm)
6	0.036	16	0.99	180
4	0.078	16	0.53	180
1	0.078	1.5	0.53	4.1

The inductance, resistance and capacitance of the power-supply net are computed using RAPHAEL, in which the Partial Equivalent Electric Circuits (PEEC) model is employed. The vias connecting Metals 6 and 4 occur at intervals along the power rails of 360 μm; we accommodate two partial self-inductance elements in this length. Thus, each of Metals 6 and 4 is represented by an inductance matrix of 930$\times$930 elements. Clearly, some simplification is needed for a solution to be achieved using a circuit simulator. In this work, the partial-inductance matrix is successively reduced by iteratively subtracting the smallest matrix term from all the other, non-zero matrix terms. For symmetrical matrices of the type considered here, this procedure is known to not affect the circuit solution [5]. We cease the reduction process when no more than four mutual inductance components are present in any column. As Fig. 2 shows, the eigenvalues of the full- and reduced-matrices match very well, except at very large eigenvalues. However, the differences have an insignificant effect on the circuit solution because the large eigenvalues correspond to the inductances of very large current loops, which carry insignificant current in the presence of smaller current loops [5].

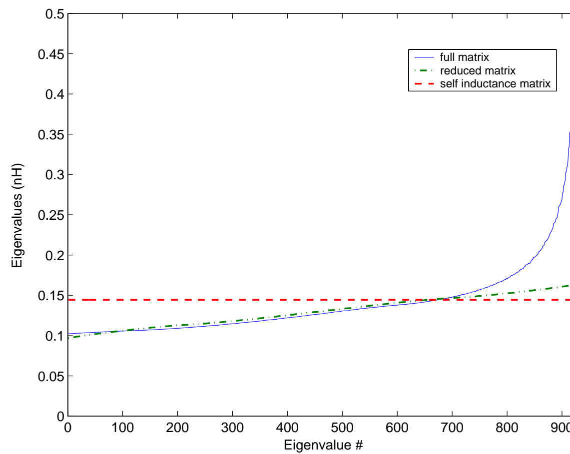

Fig. 2. Comparison of eigenvalues for the inductance matrices.

The resulting net list, which includes 12516 resistors, 1860 partial self-inductors,

and 7196 partial mutual-inductors, is incorporated into HSPICE, along with a description of the logic gates. Blocks of 10,000 gates (minimum-size inverters) are

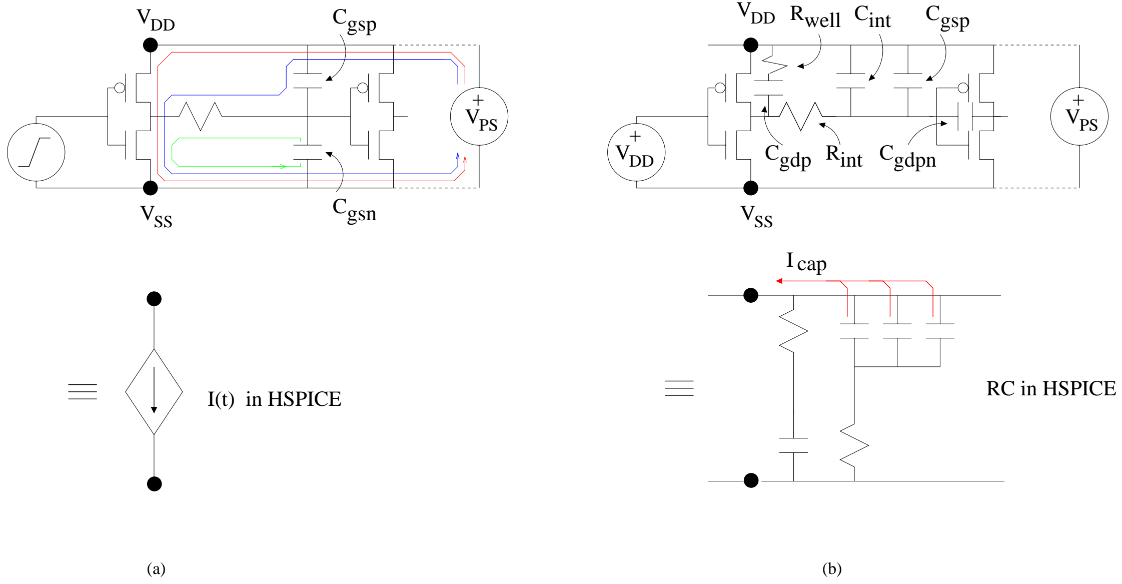

Fig. 3. Gate equivalent circuits: (a) switching gate (LO-HI transition), (b) idle gate (input HI).

placed between the Metal 1 power rails. Each gate is represented by either a current source or a series RC branch [6], as shown in Fig. 3. The current source is activated if a gate is switching. Fig. 3(a) shows three switching currents, two of which must be supplied from outside of the gate. It is these two currents that are represented in HSPICE by a time-dependent current source. The RC branch is activated if a particular gate is not switching. This description allows the current de-coupling effect of the capacitance of the idle gates to be evaluated, as illustrated in Fig. 3(b). In the equivalent-circuit representation of the idle gate, the gate-drain capacitance of the p-channel transistor in the first inverter of the gate is not considered, in view of its association with an n-well resistance R_{well}, which is large compared to the interconnect resistance R_{int} that couples the other capacitors to the power-rail node [6].

The current-source waveform for a single gate is determined from HSPICE simulations, using $0.18\,\mu$m CMOS rules, by simulating the switching of one inverter driving a similar inverter. The profile of the supply-current (I_{PS} in Fig. 1) is then generated by arranging for 20% (2000) of the gates within a block to switch at appropriate time intervals. The instant at which a gate switches is determined by Monte-Carlo procedures [2], and the locations of the switching gates are randomly distributed within the 10,000-gate block. Switching events are allowed every 50 ps, and each gate switches in 85 ps, *i.e.*, during the assumed rise-time of the local clock.

The overall switching period is 1 ns. To achieve profiles for I_{PS} which are typical of recent microprocessors [7], the number of gates forced to switch within a prescribed period (485-685 ps) is varied. In the examples shown in Fig. 4, the higher profile is produced by 1869 gates switching within the stated period, while the number for the lower profile is 1239. The respective peak currents are 43 and 25 mA, and the average currents are 4.66 and 4.59 mA. Thus, the peak-to-average ratio is about 9 for the higher-profile, which is consistent with values suggested for modern, low-power, chip design [8].

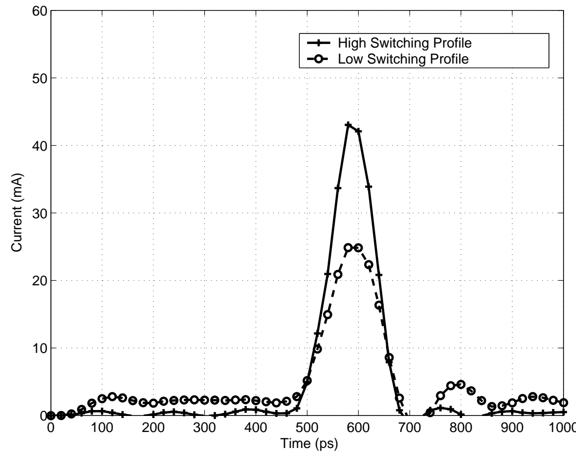

Fig. 4. Power-supply current waveforms for high- and lower-numbers of gates (1869 and 1239, respectively) switching in a 200 ps period.

Results are presented below for PSN due to various instances of switching within one core-logic block. The major objective of determining the role played by the on-chip power-net inductance is achieved by systematically increasing the complexity of the on-chip power-net impedance. First, the on-chip power net is represented merely as a resistive network. Next, the on-chip inductance is then included by separately introducing self- and mutual-inductance into the network description. For each of these cases, simulations are performed for two types of bonding, thereby allowing the relative importance of the bonding-package inductance to be assessed. Additionally, the importance of the de-coupling capacitance of the idle gates is determined by performing simulations with and without this capacitance present. Finally, by determining the PSN at a central spot in the chip due to switching in a block which can be located at various distances from this reference point, the effect of multiple blocks switching simultaneously is determined by superposition.

3. Results and Discussion

A block of 10,000, minimum-sized inverters in 0.18 μm technology occupies an area of 0.286 mm^2 [9]. When considering switching within a block, we evaluate the PSN

at one corner of the block. In all results reported here, the high-switching current profile depicted in Fig. 4 is used. For the lower-switching case portrayed in that figure, we found that the PSN scaled approximately with the magnitude of the power-supply current. This is not surprising, as a lower magnitude also means a lower rate-of-change of current in our prescription for switching. Two bonding packages were used: wire-bond and flip-chip. These represented cases of high- and low-package inductance, respectively (see below).

To illustrate the nature of the PSN, typical disturbances to V_{DD} and V_{SS}, due to switching within one block, are shown in Fig. 5. Flip-chip bonding was used in this case, and the figure shows the effect of modeling the on-chip power net as either resistive (R), resistive plus self-inductive (RL), or resistive plus self- and mutual-inductive (RLM). Clearly, the presence of the power-line inductance causes significant overshoot in both V_{DD} and V_{SS}, following the usual "droop" of V_{DD} and "bounce" of V_{SS}.

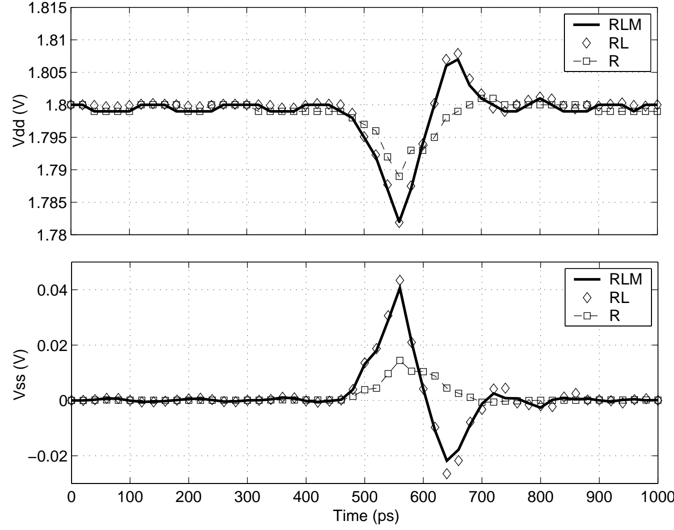

Fig. 5. Voltage waveforms: the effect of modeling the on-chip power net as either resistive (R), resistive plus self-inductive (RL) or resistive plus self- and mutual-inductive (RLM). The bonding is flip-chip and the high-switching-activity case is used.

For comparison purposes, we quantify the power-supply noise by:

$$\mathrm{PSN} = \mathrm{MAX}\{\frac{\mathrm{V_{PS} - V_{DD}(t) + V_{SS}(t)}}{\mathrm{V_{PS}}}\}, \tag{1}$$

where V_{PS} is the off-chip supply voltage. Thus, the data in Fig. 5 is summarized in Fig. 6, along with the results from employing a wire-bonded package. In the wire-bonded case, each bond pad is assumed to have an inductance of 2.3 nH and a capacitance of 27 fF [10]. In the flip-chip case, the corresponding values per bond

are 35 pH and 20 fF [10]. The flip-chip bonding scheme used here employs diagonally routed, metal lines in an additional layer (Metal 7) to connect the solder bumps. This arrangement produces five bumps per line and gives a minimum spacing between adjacent V_{DD}- and V_{SS}-bonds of 438 μm.

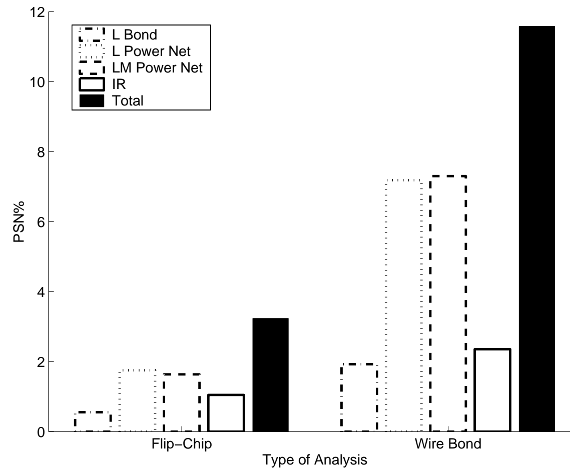

Fig. 6. PSN: the effect of the various components of the full-chip impedance network.

Figure 6 is the key figure in this paper as it shows the contribution to the PSN of each component of the full-chip impedance network. The IR case refers to the ideal situation when there is neither bonding-package inductance nor on-chip power-net inductance. The other cases shown refer to situations in which various combinations of inductance are present in a network with zero resistance. For each type of bonding package, the case labeled "total" refers to the full-chip impedance case when all resistances and inductances are modeled. It is immediately clear that the inductance of the on-chip power net is the major contributor to the PSN. This is true even in the wire-bonded case where the package inductance is high. For the flip-chip case, there is a significant ($\approx 2\times$) increase in PSN. Interestingly, the absolute increase in PSN caused by considering the power-net inductance in the wire-bond case is larger than in the flip-chip case. This indicates an interactive effect between the package- and rail-inductances that would be missed if a complete-system simulation were not performed. Thus, the PSN is higher in the wire-bond case not only because the package inductance is higher, but also because the current is forced by the end-placement of the bonds to pass through a longer length of the on-chip power net.

Regarding the effect of mutual coupling, Fig. 6 shows that when the mutual inductance components of the network are considered, there is very little change in PSN for both instances of bonding package. While some cancellation of the voltages induced by different mutual inductances is to be expected, because the cou-

pling between inductances in lines carrying similarly directed currents gives voltages that are of the opposite sense to those induced by coupling between lines carrying oppositely directed currents, we emphasize that the almost complete cancellation observed here is probably due to the particular choice of length for the partial self-inductance elements. The chosen length of 180 μm, which also applies to a partial mutual-inductance element that couples between adjacent segments on a given power line, is the same as that of the partial mutual-inductance elements coupling most directly between adjacent V_{DD}- and V_{SS}-rails. Thus, significant cancellation of voltages induced by these two sets of partial mutual-inductances can be expected. This is a very desirable situation because it means that a reasonable estimation of PSN can be obtained by considering only the partial self-inductance elements. This greatly reduces the computation time.

Having established the importance of considering power-rail inductance, we disabled the parasitic capacitance of the idle gates (see Fig. 3(b)) and repeated the above simulations with the on-chip power net represented by its resistive and inductive components. The PSN increased by $\approx$ 25%, illustrating the significant de-coupling role that is played by the capacitance of the non-switching gates within a block.

Next, we investigated the effect on PSN at our centrally located reference point within the chip of the placement of the switching block. The previous results are for the switching block located with one corner at the reference point. Fig. 7 shows results for the PSN induced at the reference point by a single switching block placed at different locations. Clearly, the influence of a switching block falls off quite rapidly

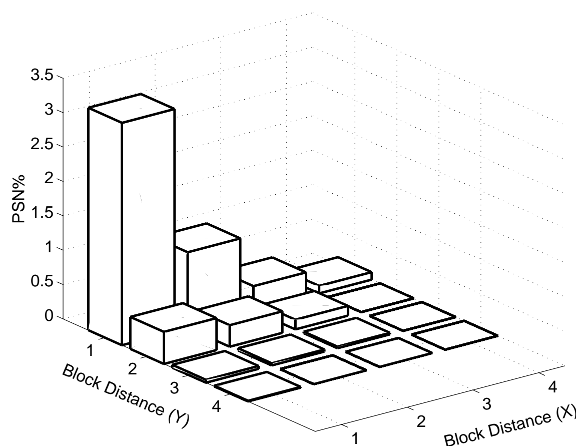

Fig. 7. PSN: the effect at the reference point (0,0.5) of the location of a switching block.

with distance from the reference point. Nevertheless, the cumulative effect of many blocks switching simultaneously cannot be ignored, as Fig. 8 reveals. For example,

four blocks, each with a corner at the reference point, conspire to produce a PSN of about 13%. This would already be unacceptable for situations with stringent PSN budgets [7,11]. Moving further out from the reference point and including the next twelve surrounding blocks causes the PSN to increase to 20%, a figure that would probably be universally unacceptable. Clearly, if such close-proximity switching is unavoidable, then the idle-gate de-coupling capacitance considered here must be augmented by additional, explicit capacitative elements in order to reduce the noise to acceptable levels [7]. Fig. 8 also shows the effect of not considering the power-rail inductance. The indications are that this would be a serious omission. For example, a PSN budget of 10% would be predicted to allow about 20 blocks to switch simultaneously, whereas, when the power-rail inductance is considered, this number drops to the much more restrictive value of three. Note that the predictions

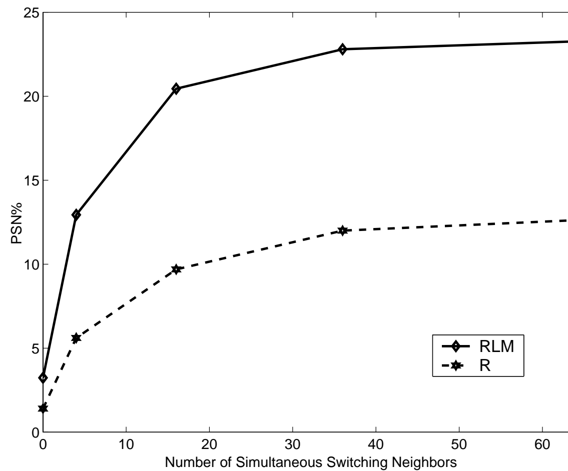

Fig. 8. PSN: the cumulative effect at the central-chip reference point of the location of additional switching blocks. The on-chip power net is modeled as either resistive (R) or resistive and inductive (RLM).

of PSN in excess of 10% should be considered with caution. This is because the current drawn by a particular block is dependent on the supply voltage, and as the voltage drops due to switching at other blocks, the current drawn by the block also decreases, thereby reducing its impact on the noise. However, for voltage variations less than about 10%, superposition should still give an accurate estimate of PSN [12].

4. Conclusions

From this systematic study by simulation of power-supply noise (PSN) it can be concluded that:

(i) PSN depends on both the bonding-package inductance and the power-rail

inductance, but even in the wire-bonded case, when the package inductance is large, the power-rail inductance is the dominant contributor to the noise;

(ii) for the flip-chip packaging case considered here, the presence of power-rail inductance increases PSN by a factor of about 2;

(iii) the de-coupling capacitance of non-switching gates in a logic block has a significant effect on PSN, but it is not likely to be large enough to realize reasonable noise budgets if more than 2 or 3 contiguous logic blocks of the type considered here are active simultaneously.

Acknowledgements

The authors are grateful to Sameer Khushal of PMC-Sierra, Inc. for valuable advice and information. Financial support from the Natural Sciences and Engineering Research Council of Canada helped make this work possible.

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