Incremental Placement Algorithm for Field Programmable Gate Arrays

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Contributions

• Incremental Placement Algorithm
  – RePlace
  – Based on Placement Locality and Floor-planning
  – Multi-Region Algorithm

• Incremental Benchmark Circuits
  – Synthetic Benchmark Set
  – Physical Re-Synthesis Benchmark Set

• Findings
  – 50-260x speed up for Single-Region Benchmarks
  – 50-70x speed up for Multi-Region Benchmarks
Motivation

- **Runtime for placement is increasing with increasing FPGA sizes**
  - 6 hours for 50,000 LUT circuit
  - Time == Engineering Cost
- **System-on-Chip circuits are made of many subcomponents**
- **What if one part is modified?**
  - Component reuse and hierarchy
  - Multiple regions of the circuit need incremental placement in order to support reuse
  - Floor-planning for each circuit
- **Physical Re-Synthesis Flows**
Incremental Placement Challenges

- Example:
  - C4, C5, D4, D5 is a modified sub-circuit
  - Can only fit \( \leq 4 \) CLBs in the previous location
  - Free space is far away!
  - How do we fit \( >4 \) CLBs quickly?
RePlace Formulation

• Placement Locality
  – Modified Sub-Circuits should be “close” to previous location
  – Floorplans

• Expanded “Virtual” Placement Grid
  – Literally thinking outside of the box!

• Efficient Shifting Algorithm
  – No CPU Intensive LE/CLB swapping and cost evaluation
RePlace Algorithm

Four Steps to Incremental Placement

1. Previous Placement and Floor-planning
2. Expanded “SuperGrid” Placement
3. Compaction Re-legalization
4. Simulated Annealing Refinement
Previous Placement and Floor-planning

```
  1   2   3   4   5   6   7
IO   IO   IO   IO   IO   IO   IO
  1   a2  a3  a4  a5  a6  IO
IO   b2  b3  b4  b5  b6  IO
  3   c1  c2  c3  c4  c5  c6  IO
IO   d1  d2  d3  d4  d5  d6  IO
  5   e1  e2  e3  d4  e5  e6  IO
IO   f3  f4  f5  f6  IO
```

Red squares indicate the areas that are highlighted.
Expansion Phase (SuperGrid)
Compaction Phase
## Intermediate Solution

<table>
<thead>
<tr>
<th></th>
<th>a2</th>
<th>a3</th>
<th>a4</th>
<th>b5</th>
<th></th>
<th>a6</th>
</tr>
</thead>
<tbody>
<tr>
<td>b2</td>
<td>b3</td>
<td>b4</td>
<td>i7</td>
<td>a5</td>
<td>b6</td>
<td></td>
</tr>
<tr>
<td>c1</td>
<td>c2</td>
<td>c3</td>
<td>i1</td>
<td>i2</td>
<td>i5</td>
<td></td>
</tr>
<tr>
<td>d1</td>
<td>d2</td>
<td>d3</td>
<td>i4</td>
<td>c6</td>
<td>d6</td>
<td></td>
</tr>
<tr>
<td>e1</td>
<td>e2</td>
<td>e3</td>
<td>d4</td>
<td>i3</td>
<td>i6</td>
<td></td>
</tr>
<tr>
<td>f3</td>
<td>f4</td>
<td>f5</td>
<td>f6</td>
<td>e5</td>
<td>e6</td>
<td></td>
</tr>
</tbody>
</table>
Simulated Annealing Refinement

• Retuned VPR Simulated Annealing Algorithm
  – Lower Initial Temperature (44% temp)
  – Smaller Range Window
  – Lower Temperature degradation factor (Alpha)
  – Variable number of swaps per temperature range, 1-3x number of CLBs
Benchmarking

• Two Benchmark Sets

• Single Region:
  – Synthetic Flow
    • Simulates a design change

• Multi Region:
  – Physical Re-Synthesis flow
    • Circuit unchanged, clustering or tech-mapping changed for optimizations
    • Scaled to select multiple regions
Single Region Synthetic Benchmark Set (SR)

- Developed by Dave Grant
- Select a rectangular region on the placement grid
  - Replace it with a synthetic clone
  - Clone can be same size, smaller, or larger (double size)
- Selection region of 2.5%, 5%, 10% of array size
## SR: Run-Time Results

<table>
<thead>
<tr>
<th>Synthetic Circuit</th>
<th>Syn - 2.5</th>
<th>Syn - 5</th>
<th>Syn - 10</th>
<th>Syn - 2.5d</th>
<th>Syn - 5d</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLMA</td>
<td>72.0</td>
<td>70.8</td>
<td>73.5</td>
<td>80.3</td>
<td>70.0</td>
</tr>
<tr>
<td>EX1010</td>
<td>77.6</td>
<td>75.0</td>
<td>77.0</td>
<td>69.0</td>
<td>76.2</td>
</tr>
<tr>
<td>MISEX33</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>PDC</td>
<td>80.6</td>
<td>64.0</td>
<td>68.7</td>
<td>84.4</td>
<td>68.1</td>
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<tr>
<td>SPLA</td>
<td>75.7</td>
<td>55.5</td>
<td>44.8</td>
<td>84.0</td>
<td>51.2</td>
</tr>
</tbody>
</table>

**Geometric Mean:** 70.1
SR: Channel Width Results
Multi-Region Physical Resynthesis Benchmark (MR)

- Un/DoPack developed by Marvin, Guy and myself
- Iterative Congestion Reduction Algorithm
  - Select congested region
  - Spread out LUTs by adding whitespace to each CLB
- Multiple Regions
- Select all regions needed to reduce CW by 10%, 20%, 30%, 40%, 50%
- 1/3 to 2/3 of the entire FPGA re-synthesized
# MR: Run-Time Results

<table>
<thead>
<tr>
<th>Multi-Region Circuit</th>
<th>MR - 50</th>
<th>MR - 40</th>
<th>MR - 30</th>
<th>MR - 20</th>
<th>MR - 10</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLONE</td>
<td>62.8</td>
<td>70.0</td>
<td>68.3</td>
<td>61.5</td>
<td>75.9</td>
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<tr>
<td>STDEV0</td>
<td>67.3</td>
<td>66.8</td>
<td>55.1</td>
<td>56.0</td>
<td>66.3</td>
</tr>
<tr>
<td>STDEV010</td>
<td>47.1</td>
<td>59.7</td>
<td>68.6</td>
<td>66.5</td>
<td>58.5</td>
</tr>
</tbody>
</table>

**Geometric Mean**

63.0
MR: Channel Width Results

![Graph showing MR: Channel Width Results](image-url)
MR: Critical Path Results
Contributions

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Future Works

• Support for Macro Blocks
• Support for Carry Chains
• More Intelligent Shifting
  – Still keep it simple
• Integration with Commercial flows
  – EG: QUIP
End of Talk,
Thank you!!
Questions?