PCB Design support for ELEC391:

Altium 2016, 150 licenses

Lecture talks:

• Jan 30 Altium I (Design Capture + Simulation)
• Feb 6   Altium II (PCB Layout)
• Mar 13 Guest Lecture – PCB Production
• Support & submission instructions posted [here](#)

Mechanical and PCB design support available 2hrs per lab session, rooms MCLD315,306
- Mon: 13:00-15:00 / 16:00-18:00
- Tue: 09:00-11:00 / 12:00-14:00 / 16:00-18:00
- Wed: 13:00-15:00 / 16:00-18:00
- Tue: 09:00-11:00 / 12:00-14:00 / 16:00-18:00
Contents

• How to install Altium Designer 2016
• Understanding Altium Designer
• Walk-through Tutorial
  – Schematic Capture
  – Mixed signal simulations
• SPICE basic concepts

Credits: Unless explicitly stated all source material is from the Altium website and Altium training documents.
Typical PCB Design flow

Front-end design and capture

Back-end design

- Conceptual Idea
- System Definition
- Schematic Capture
- PCB Layout
- Debug/Test
- Final Product
- Mixed-signal circuit simulation
- Pass
- Fail

http://e2e.ti.com/
Typical PCB Design flow

Front-end design and capture

1. Conceptual Idea
2. System Definition
3. Schematic Capture
   - Mixed-signal circuit simulation
4. PCB Layout
5. Debug/Test
6. Final Product
7. Pass
8. Fail
9. Generate CAM files
10. Fabricate
11. Populate

http://e2e.ti.com/
Altium Designer 2016
A complete product development system

System requirements (MS W7, W8, W10)

- Front-end design and capture
- Physical PCB design
- FPGA hardware design
- FPGA system implementation and debugging
- Embedded software development
- Mixed-signal circuit simulation
- Signal integrity analysis
- PCB manufacturing
How to install Altium 2016

• Link to our download site:
  https://download.ece.ubc.ca

• Useful links:
  http://www.ece.ubc.ca/~leos/pages/tools/altium.html

• Create an account at Altium Live:
  http://live.altium.com/#signin_ (slow)
  email: engservices@ece.ubc.ca (fast)
Install .zip file

**Electronic Software Distribution**

**ALTUIM DESIGNER**
Circuit Design Software

**External Links**
- Altium
- Altium Designer

**ALTUIM DESIGNER 16**

<table>
<thead>
<tr>
<th>File</th>
<th>Size</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>README.html</td>
<td></td>
<td>README</td>
</tr>
<tr>
<td>AltiumDesigner16Setup.exe</td>
<td>10.4 MB</td>
<td>Windows installer (requires)</td>
</tr>
<tr>
<td>EULA.pdf</td>
<td>56.2 KB</td>
<td>End-User License Agreement</td>
</tr>
<tr>
<td>OfflineSetupAD16_1_9.zip</td>
<td>3 GB</td>
<td>Windows installer</td>
</tr>
</tbody>
</table>

**Using the ECE License Server**

The ECE license server for Altium is accessible only from the UBC network. Before starting Altium, you should be connected by one of the following means:

- A wired connection on the ECE network
- A wired connection on UBC ResNet
- A wireless connection at the UBC Vancouver campus on the ubcprivate, ubcsecure, or ubc network (ubcvisitor and eduroam are not sufficient)
- A myVPN connection to the UBC Vancouver network
- A myVPN connection to the ece.prof pool

Start Altium, and from your "My Account" page, click on "Setup private license server". Enter:

- Server name:
- Server port:
- Secondary server name:
- Server port:

Select the new license that appears and click on "Use". You may as well also delete any old, expired licenses that are also showing.
To set license server

As per README.html file

If you loose connection to server click here:

As per README.html file
Understanding Altium

• DXP (Design explorer): Unified platform
• Collaborative environment (corporate tool):
  – Multiple users, some with dedicated tasks
  – Design team incremental changes day-by-day
  – Built-in version control (SVN subversion or CVS concurrent versions system)
  – Design repositories / Vaults (accessible by multiple users with different credentials)
• Cloud oriented:
  – Save preferences
  – http://live.altium.com/ (forum, design content, blog)
Altium Design Environment

System Menu
Access to features including environment preferences and server information.

Menus/Toolbars/Shortcuts
Resources change according to the active document editor.

Document Tabs
Each open document has its own tab. Click on a document tab to make it the active document. Right-click on a tab for further controls.

Navigation
Provides controls for jumping to a particular document, stepping back and forth through viewed documents, and accessing the Home page.

Workspace Panels
Various panels provide functionality specific to a particular editor, or at a system level. Panels can be docked, placed in a 'pop-out' mode, or floating.

Main Design Window
Display and arrange open documents in this window.

Panel Access
Workspace panels are accessible using these buttons.
Recommended basic panels

For more help working with panels read this
Understanding Altium
(Basics for the single user)

Don't forget:

• Use Keyboard shortcuts
  <Shift + F1> while running a command
• <Esc> or Right Click to exit a command
• Save documents to see some changes take effect
Understanding Altium
(Basics for the single user)

- **Projects** (project panel, active project)
- **Workspace Panels** (system-wide, editor-specific)
- **Editors:**
  - Schematic
    - Symbol editor
  - PCB layout
    - Footprint editor
    - CAM files (CAMtastic panel)
- **Components and Libraries**
Altium Projects

- Project: collection of design documents
  - 1 Project = 1 implementation
  - It stores links to all source documents
    - relative reference: same drive
    - absolute reference: different drive
  - It creates links to all output documents
  - Saves project options
- Create a PCB_Project, Save as: new name
  (does not move the file creates a copy)
- The active project is highlighted
- Add/Remove documents to/from a project
Altium Projects: types

- PCB Project (*.PrjPcb)
  - Schematic, libraries, PCB layout
- FPGA Project (*.PrjFpg)
- Embedded Project (*.PrjEmb)
- Core Project (*.PrjCor)
- Integrated Library (*.LibPkg) & (*.IntLib)
- Script Project (*.PrjScr)
Component, Model and Library Concepts

- Component representations:
  - Schematic symbol
  - PCB footprint
  - SPICE model definitions
  - Signal integrity description
  - 3D graphical description
Component, Model and Library Concepts

• Domains = Different phases of design
  – Schematic capture
  – PCB layout (2D / 3D)
  – SPICE simulation
  – Signal integrity analysis

• A unified component is a container with links to all domain models + parametric information
Libraries = collection of components

- Collection of components, models or both
- Model Libraries (*.MDL, *.CKT, *.PCBLib)
  - Simulation models are one file per model
- Schematic Libraries (*SchLib)
  - Symbol and a link to a model library
- Integrated Libraries (*.IntLib)
  - Symbol, footprint and other models are compiled into a single portable file
Project: part of and available only to the active project and its documents. You have to keep track of where these are if you move the project files.

Installed: All installed libraries. Components are available to all open projects and list is persistent across design sessions.

Search Path: Additional Libraries accessible via a search path and sub-folders. The search paths are valid for the active project.
Libraries Panel:

All libraries available to the active project

- Project + Installed + Search
- Path

When placing component:

- <spacebar> to rotate
- <x> or <y> to flip
- <Tab> open properties dialog
- <L> for PCB footprints to flip component side

To search across libraries:

- Search …
Obtaining integrated libraries

1. **Frozen (legacy) libraries:** from here you can install anywhere but it is a good idea to make a subfolder under:
   C: \ Users \ Public \ Public Documents \ Altium \ AD16 \ Library
   or a cloud storage service if you work from more than one PC

2. **AltiumLive website:** Resources / Design Content

This is useful to preview component

This downloads a .zip file for the complete library
Altium Vault

Altium’s cloud library (repository of models)
Also includes real-time supply chain information
Learning to use Altium

Best training material is on the Altium website. It is updated, but beware that menus and options slightly change between versions.
Demo: Schematic entry and Simulation

http://techdocs.altium.com/display/AMSE/Defining+&+Running+Circuit+Simulation+Analyses

Miscellaneous Devices.IntLib
{Res1, Cap}

NSC Amplifier.IntLib
{LF411CN} flip in Y!

Vin
Amplitude = 5V
Frequency = 50KHz

Vsin
Value = 5V

Vscr
Value = 5V

Vscr
Value = -5V
Set simulation parameters
Set simulation parameters

### Transient Analysis Setup

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transient Start Time</td>
<td>0.000</td>
</tr>
<tr>
<td>Transient Stop Time</td>
<td>60.00u</td>
</tr>
<tr>
<td>Transient Step Time</td>
<td>100.00n</td>
</tr>
<tr>
<td>Transient Max Step Time</td>
<td>200.0n</td>
</tr>
</tbody>
</table>

### AC Small Signal Analysis Setup

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Start Frequency</td>
<td>100.0m</td>
</tr>
<tr>
<td>Stop Frequency</td>
<td>1.000meg</td>
</tr>
<tr>
<td>Sweep Type</td>
<td>Decade</td>
</tr>
<tr>
<td>Test Points</td>
<td>100</td>
</tr>
</tbody>
</table>
Wiring Tips

- Left-click or <Enter> to anchor the wire at the cursor position.
- <Backspace> (←) to remove the last anchor point.
- <Spacebar> to toggle the direction of the corner.
- <Shift+Spacebar> to cycle through all possible corner modes.
- Right-click or <Esc> to exit wire placement mode.
- To graphically edit the shape of a wire, Click once to select it first, then Click and hold on a segment or vertex to move it.
- Whenever a wire crosses the connection point of a component, or is terminated on another wire, a junction will automatically be created.
- A wire that crosses the end of a pin will connect to that pin, even if you delete the junction.
- To move a placed component and drag connected wires with it, hold down the Ctrl key while moving the component, or select Move » Drag.
About SPICE

• Berkley (class project +Masters),  CANCER Computer Analysis of Nonlinear Circuits Excluding Radiation

• Berkley (PhD) , Simulation Program with Integrated Circuit Emphasis
  → SPICE 1972 FORTRAN
  → SPICE 2 1975, SPICE 2G6 1983
  → SPICE 3 1989 C, SPICE 3F5 1993
  → SPICE 4 2004 (RF)

• Proprietary versions of SPICE
  SPICE-like simulators or “Alphabet SPICE”
  HSpice, XSPICE (Georgia Tech), PSPICE, etc
Altium and SPICE

• Altium Designer is compatible with:
  – SPICE3f5 (Berkley SPICE)
  – XSPICE (Georgia Tech)
  – PSPICE (Micro/Sim/Orcad/Cadence)

• You may need to change the file extension to .mdl or .ckt

```
.MODEL Diode D
+(  AF=1.0  Bv=5.2  CJO=0.0  EG=1.11  FC=0.5  Ibvl=0.2  Ibv=5  Ikf=10  IS=1E-14
   Isr=1.8n  KF=0.0  M=0.5  N=1.0  Nbv=3.1779  NBVL=1.0  Nr=1.5  Rs=.5875
   TBV1=0.0  TBV2=0.0  TIKF=0.0  TRS1=0.0  TRS2=0.0  Vj=.75  XTI=3.0
+)
```

SUBCKT / .ENDS

• Other models need to be manually converted!
SPICE Models and Subcircuits

.SUBCKT LF411/NS 1 2 99 50 28
*
**************************INPUT STAGE**************************
*
IOS 2 1 25.0P
*^Input offset current
CI1 1 0 3P
CI2 2 0 3P
R1 1 3 1E12
R2 3 2 1E12
I1 99 4 1.0M
J1 5 2 4 JX
J2 6 7 4 JX
R3 5 50 650
* etc,etc...
* Code truncated to demonstrate concept
* Refer to http://www.national.com/models/spice/LF/LF411.MOD
* For complete .ckt file of the LF411/NS model
************************** LOCAL MODELS USED**************************
*
.MODEL JX PJF(BETA=1.183E-3 VTO=-.65 IS=50E-12)
*
*Note that Model JX is referenced in the .SUBCKT
*by the J2 device.
.ENDS LF411/NS
SPICE Netlist

- Subcircuits, models + analysis command + graphical output settings

*SPICE Netlist generated by Advanced Sim server

Cload 0 LLTRA_OUT 10pF
TLLTR1 LLTRA_IN 0 LLTRA_OUT 0 Z0=75 TD=19.6ns
Rload 0 LLTRA_OUT 75
Rs LLTRA_IN VS 5
Vinu$put VS 0 DC 0vdc$m PWL(0U 0V 10ns 2V 300ns 2V) AC 1vacm 0

.SAVE 0 LLTRA_IN LLTRA_OUT VS Vinput#branch @Vinput[z] @Cload[i] @Rload[i] @Rs[i]
.SAVE @Cload[p] @Rload[p] @Rs[p] @TLLTR1[p] @Vinput[p]

*PLOT TRAN -1 1 A=LLTRA_IN
*PLOT OP -1 1 A=LLTRA_IN

*Selected Circuit Analyses:
.TRAN 1.2E-9 3E-7 0 1.2E-9
.OP

.END

Asterisks (*) = Comments, Plus (+) = Line continuation, Period (.) = Command
Letters (A to Z) are used to represent elements, D= Diode, R = Resistor etc.
# SPICE Syntax Reference (1/2)

<table>
<thead>
<tr>
<th>Letter</th>
<th>Device</th>
<th>Syntax</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Xspice / SimCode</td>
<td>Digital SimCode models</td>
</tr>
</tbody>
</table>
| B      | Non-Linear Dependent Voltage Source | B<refdes> <+node> <-node> V=<EQUATION>  
EQUATION denotes the expression defining the source waveform |
<p>| C      | Capacitor                      | C&lt;refdes&gt; &lt;+node&gt; &lt;-node&gt; [&lt;model&gt;] &lt;value&gt; [IC=&lt;initial voltage&gt;]     |
| D      | Diode                          | D&lt;refdes&gt; &lt;+node&gt; &lt;-node&gt; &lt;model&gt; [AREA] [IC=&lt;initial voltage&gt;] [TEMP=&lt;temperature&gt;] |
| I      | Current Source                 | I&lt;refdes&gt; &lt;+node&gt; &lt;-node&gt; [[DC] &lt;value&gt;] [AC &lt;magnitude&gt; + [&lt;phase&gt;]]   |
| J      | Junction FET                   | J&lt;refdes&gt; &lt;drain&gt; &lt;gate&gt; &lt;source&gt; &lt;model&gt; [area] [initial on/off starting condition] [IC=initial D-S voltage, initial G-S voltage] |
| K      | Inductor Coupling              | K&lt;refdes&gt; L&lt;name1&gt; &lt; L&lt;name2&gt; &gt; &lt;coupling&gt;                              |
| L      | Inductor                       | L&lt;refdes&gt; &lt;+node&gt; &lt;-node&gt; [model] &lt;value&gt; [IC=&lt;initial current&gt;]        |</p>
<table>
<thead>
<tr>
<th>Letter</th>
<th>Device</th>
<th>Syntax</th>
</tr>
</thead>
<tbody>
<tr>
<td>M</td>
<td>Mosfet</td>
<td>M&lt;refdes&gt; &lt;drain&gt; &lt;gate&gt; &lt;source&gt; &lt;substrate&gt; &lt;model&gt; + [L=&lt;value&gt;] [W=&lt;value&gt;] + [AD=&lt;drain area value&gt;] [AS=&lt;source area value&gt;] + [PD=&lt;drain perimeter value&gt;] [PS=&lt;source perimeter value&gt;] + [NRD=&lt;value&gt;] [NRS=&lt;value&gt;] + [IC=&lt;initial D-S volt.&gt;, &lt;initial G-S volt.&gt;, &lt;initial B-S volt.&gt;] + [TEMP=&lt;temperature&gt;]</td>
</tr>
<tr>
<td>Q</td>
<td>Bipolar Transistor</td>
<td>Q&lt;refdes&gt; &lt;collector&gt; &lt;base&gt; &lt;emitter&gt; &lt;model&gt; [&lt;area&gt;] + [IC=&lt;initial B-E voltage&gt;, &lt;initial C-E voltage&gt;] + [TEMP=&lt;temperature&gt;]</td>
</tr>
<tr>
<td>R</td>
<td>Resistor</td>
<td>R&lt;refdes&gt; &lt;+node&gt; &lt;-node&gt; [&lt;model&gt;] &lt;value&gt;</td>
</tr>
<tr>
<td>S</td>
<td>Voltage controlled switch</td>
<td>S&lt;refdes&gt; &lt;+node&gt; &lt;+node&gt; &lt;+control&gt; + &lt;+control&gt; &lt;model&gt; [initial condition]</td>
</tr>
<tr>
<td>T</td>
<td>Transmission Line</td>
<td>T&lt;refdes&gt; &lt;A+&gt; &lt;A-&gt; &lt;B+&gt; &lt;B-&gt; Z0=&lt;value&gt; + [TD=&lt;value&gt;</td>
</tr>
<tr>
<td>V</td>
<td>Voltage Source</td>
<td>V&lt;refdes&gt; &lt;+node&gt; &lt;+node&gt; [[DC] &lt;value&gt;] + [AC &lt;magnitude&gt; [&lt;phase&gt;]]</td>
</tr>
<tr>
<td>X</td>
<td>Sub-circuit call</td>
<td>X&lt;refdes&gt; [&lt;node&gt;]* &lt;sub-circuit name&gt;</td>
</tr>
<tr>
<td>Unit Multiplier</td>
<td>Value</td>
<td>Nomenclature</td>
</tr>
<tr>
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<td>--------------</td>
</tr>
<tr>
<td>T</td>
<td>$10^{12}$</td>
<td>Tera</td>
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<td>$10^{9}$</td>
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<td>$10^{3}$</td>
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<td>$25.4^{-6}$</td>
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<tr>
<td>f</td>
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<td>Femto</td>
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