Ultra-Low Power 90nm 6T SRAM Cell for Wireless Sensor Network Applications

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Abstract—This paper presents a comparative study of leakage reduction techniques applied to a 90nm 6T SRAM to find an optimal design for ultra-low power wireless sensor applications. A 4-Kb SRAM implemented with the proposed techniques has a leakage as low as 26.5nA in the idle mode, a 189X improvement over a memory without applying such techniques.

I. INTRODUCTION

The emerging Wireless Sensor Network technologies are facilitating novel applications in health monitoring, industrial monitoring and security surveillance. The small physical dimensions of wireless sensor nodes often restrict the energy source to a small battery. The limited energy consumption requirement demands for ultra-low power sensing, processing and communication. Ultra-low power approaches at the device, circuit, system and network level have been proposed for reliable implementations of sensor networks [1-3].

SRAM, being a key component of the processing system of sensor nodes, has to satisfy the low-power requirement as well. As feature size shrinks, the key component of power consumption will be leakage [4]. In the past 5 years, there has been significant effort to find ways to reduce leakage, amongst them are supply voltage scaling [5, 6], idle mode implementation [7-9], and body biasing [5, 10]. While the existing solutions provide good leakage reduction, they mostly target microprocessor cache, with circuit performance being a critical parameter to be optimized. This limits the extent to which leakage reduction techniques can be applied, rendering them ineffective for the ultra-low power domain. In a sensor node, there are two modes of operation, namely data processing and idle. Since the memory spends almost its entire operating time in the idle mode, it is critical to vastly reduce leakage while retaining data. With the primary function of retaining data and speed being only a secondary requirement, good cell stability, reflected by a high Static Noise Margin (SNM), becomes a critical design objective for a SRAM used in a wireless sensor application.

This paper compares leakage reduction techniques applied to the 6T SRAM cell implemented in a 90nm technology to find an optimal design for ultra-low power wireless sensor applications primarily from a power perspective. The techniques include the use of multi-VT transistors, scaling supply voltage, sizing above minimum gate length, and implementing sleep transistors. The leakage reduction ability and the corresponding sacrifice in SNM of each technique are compared. Section II examines major sources of leakage present in the 6T cell. Section III describes the impact of the supply voltage and the transistor threshold values on leakage. Section IV analyzes the effect of transistor sizing on leakage. Section V investigates the effectiveness of sleep transistors in leakage reduction, followed by a comparison and conclusion in Section VI.

II. 6T SRAM LEAKAGE ANALYSIS

The standard 6T SRAM cell is shown inside the box in Figure 1, with M₅ and M₆ normally connected to ground rather than to Msleep (Msleep included only in Section V simulations). M₂ and M₄ are the access transistors for read and write operations. M₁₄ form a cross coupled inverter with positive feedback to statically retain data.

![Figure 1](image)

**Figure 1** The standard 6T SRAM cell with the addition of a sleep transistor.

To clarify the leakage sources in the cell, assume V₁ and V₂ are biased to a logic zero and a logic one respectively. Thus M₁ and M₄ are turned off. M₂ and M₃ give rise to the leakage currents Iₛ₁ and Iₛ₂ respectively. Iₛ₁ and Iₛ₂ form the supply leakage as they drain charges from the supply grid.

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The access transistors are off when the wordline (WL) is not selected (idle mode). Since the bitlines are precharged to VDD when the memory is idle, M5 and M1 both leak. However, since V2 and BIT’ are high, resulting in a very small voltage difference between the drain and source of M6, leakage through M6 is typically only in hundreds of femto-amperes. Hence it can be reasonably ignored. The leakage of M5 (IB1) forms the bitline leakage. Based on the above definition of leakage components, applying leakage reduction techniques to the PMOS transistors reduces supply leakage and doing the same for the access transistors reduces bitline leakage. Simulations confirm that applying leakage reduction techniques to the inverter pull-down network reduces both leakage components.

In this paper, we study the stability of the cell by measuring the SNM. SNM is the minimum amount of noise that can corrupt the data stored in the cell. For SNM simulations, noise sources are added to the inputs of both inverters with the worst case polarity as shown in Figure 2 [5]. Simulations are performed at 25 ºC and all transistors have L = 100nm, which is the minimum feature size for the 90nm technology used. The access transistors have W = 140nm and the inverters have Wp/Wn = 180nm/200nm for correct write and read operations [5].

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### Figure 2 Noise Model in the cell [5].

III. Leakage Reduction by Supply Voltage Scaling and High Threshold Transistors

Supply voltage scaling is a well known method to reduce the power consumption of a circuit. The leakage is reduced due to smaller voltage differences between the drain, source and body of a transistor.

As depicted in Figure 3a, the leakage current through the supply and the bitlines of the SRAM cell is significantly reduced for low supply voltages (e.g. 0.2V). It also shows that a cell with higher threshold voltages has significantly lower leakage even at a nominal supply voltage of 1.2V. Figure 3b shows that cell stability is compromised as supply voltage is lowered.

### Figure 3 Leakage reduction achieved by supply voltage scaling and high threshold transistors: (a) Leakage reduction by supply voltage scaling, (b) cell stability trade off in terms of lowered SNM. Results are shown for high, standard, and low threshold transistor implementations (HVT, SVT, and LVT respectively).

IV. Leakage Reduction by Size Scaling

Transistor sizing is a simple yet effective way to reduce leakage. Figure 4 depicts the tradeoff between area and leakage reduction. Gate dimensions, W and L, are scaled by a factor S. In our first case study, W and L are scaled at the same time to keep the same aspect ratio and in the other case, only L is scaled. When W and L are scaled together by S, we see two key leakage components at work: subthreshold leakage (between source and drain) and junction leakage (between drain and body) [9]. Both supply and bitline leakage initially decrease rapidly due to reduction of the subthreshold component. But as S becomes larger, the subthreshold component becomes comparable to the junction component, which strongly depends on W. Considering that the total area used by the access transistors
is relatively small, it is effective to scale them more aggressively than inverters. A reasonable choice is \( S = 1.1 \) for the inverters and \( S = 1.2 \) for the access transistors. In this case, supply and bitline leakage are 20.2pA (66% of total cell leakage) and 10.2pA (34%) respectively, for a total of 30.4pA per cell.

V. LEAKAGE REDUCTION BY SLEEP TRANSISTOR

A sleep transistor can be implemented between ground and the node (GNDX) that connects to the sources of all pull-down NMOS transistors within a column in the memory array, as shown in Figure 1. This circuit topology introduces the stack effect, also present in the pull-down network of a NAND gate [9]. The upper portion of the stack is the parallel combination of all pull-down NMOS transistors while the lower portion is the sleep transistor. Due to the leakage current through the stack, GNDX is above ground level, causing the gate-to-source voltage of the pull-down NMOS transistors to be negative when their gates are at logic zero. The sleep transistor has leakage \( I_{\text{Sleep}} \), which is the total leakage of a column. In the idle mode, the sleep transistor’s control input \( V_C \) is low, disconnecting the memory cells from ground. When the cell is active, \( V_C \) is high, providing a path that connects the cells to ground with ideally low resistance. The choice of an NMOS instead of a PMOS as the sleep transistor is due to the fact that both supply and bitline leakage current flow through the pull-down network.

Figures 5a and 5b show respectively the dependencies of the supply and the bitline leakage on the size of a high threshold voltage (HVT) sleep transistor. We propose the use of HVT as other \( V_T \) levels reduce leakage by such a small amount that its benefit does not outweigh the additional circuit complexity. With a 1.2V \( V_{DD} \), SNM is obtained for different numbers of 6T cells attached to the column of the memory array as depicted in Figure 6. SNM is significantly lowered by the sleep transistor. For comparison, the implementation without the sleep transistor yields an SNM of 475mV as shown in Figure 3b. The loss of SNM is compensated by a large leakage reduction.

To achieve a particular SNM, the size of the sleep transistor must be scaled linearly with respect to the number of cells in a column. As can be observed in Figure 6, it takes a sleep transistor with 1µm of width to achieve a SNM of 100mV for the 1-cell case. It takes 2µm and 4µm for the 2-cell and 4-cell case respectively to achieve the same 100mV SNM. Contrary to SNM, the leakage does not scale linearly. The leakage per cell decreases as the number of cells in a column increases as observed in Figure 5. For example, using a 10µm sleep transistor, the bitline leakage for 1 cell is 23pA while the bitline leakage for 16 cells is just 62pA. This result suggests that greater leakage reduction can be achieved with a large sleep transistor when the number of cells in a column is large. The supply voltage scaling technique does not exhibit this characteristic.

In an attempt to further reduce leakage, two NMOS sleep transistors are stacked between GNDX and circuit ground as in Figure 1. Figure 7a and 7b shows supply and bitline leakage respectively when stacking two sleep transistors. Examining solely the leakage reduction, by comparing Figure 5 and 7, the sleep transistor stack is a superior implementation. However, the SNM of the transistor stack implementation is noticeably worse than the case with only one NMOS sleep transistor due to the high resistance path between GNDX and circuit ground. Using SNM as a cross reference, that is using the two methods to achieve a specified SNM, we find that the use of two stacked NMOS sleep transistors yields less leakage reduction; hence the single NMOS implementation is preferred.
VI. CONCLUSION

Different leakage reduction techniques were applied and compared to the 6T SRAM cell to yield optimal leakage reduction while maintaining acceptable cell stability. This work investigated the use of different $V_T$ transistors, scaling supply voltage, sizing above minimum gate length, and implementing single and stacked sleep transistors. The counterintuitive results suggest that, after scaling transistors beyond minimum gate length, sleep transistor implementation yields greater leakage reduction than supply voltage scaling. While the wealth of existing knowledge mainly targets cache memory, the proposed combinations of techniques are effective in the emerging ultra-low power wireless sensor network domain. Proper applications of these techniques can reduce leakage by 189X for a 4Kb SRAM assuming 64 cells per column, with further reduction for a larger size memory. Future work may investigate the performance impact of leakage reduction techniques so that a power-performance tradeoff can be made.

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REFERENCES


