Low Phase Noise 1GHz Digitally Controlled Quadrature Ring Oscillator in 0.18 \( \mu m \) CMOS Technology

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This paper presents a 14-bit digitally controlled ring oscillator (DCO) with operating frequency up to 1 GHz in 0.18 \( \mu m \) CMOS technology. Digital control is employed for controlling transistor operation to obtain higher voltage swing and lower flicker (1/f) noise that in turns results in the lowest phase noise in ring oscillator.

Fig. 1(a) shows a general topology of the proposed digitally controlled quadrature ring oscillator. The schematic of delay cell is shown in Fig. 1(b). In a delay cell, transistors M1 and M2 act as digital inverter with equal slew rate both on rising and falling edges. Meanwhile, transistor pairs M3, M4 and M5 serve as transition-assistance transistors. M5 is used to control the voltage on M3 drain by varying its gate voltage. The size of M3 is made very large compared to M4 and M5, but the size of M4 and M5 cannot be too small since it has to pull the voltage at M3 drain. The value of the M3 has to be optimized to get the maximum output frequency. The design is implemented in 0.18 \( \mu m \) CMOS technology as the chip photo is shown in Fig. 2.

Fig. 3 shows the measured phase noise of DCO where the measured phase noise was -123 dBC/Hz at 1 MHz offset of 1 GHz carrier frequency, which is comparable to a recently reported value for Inductor-Capacitance (LC)-type oscillator [1]. The DCO has a frequency tuning from 212 MHz to 1.01 GHz.

The better phase noise performance and scalability makes DCO suitable for reconfigurable wireless and wired ADPLL applications.

Fig. 1(a) General topology

(b) Delay cell circuit.

Fig. 2. Chip photo (Size in mm²)

Fig. 3. Measured phase noise